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Optimization of Fully-Differential Folded Cascode Amplifier via Multi-Objective Genetic Algorithms

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***Abstract*— The miniaturization of advent Microsystems largely complicated the task of the designers. So design an interface to an application specific sensor induces costs and design time high mainly related to the analog part. To reduce these costs should have been standardized design analog like digital electronics and everyone knows the delay in the analog domain. The methodology presented in what follows aims to reduce the gap and allows automated synthesis of analog and mixed systems. It is a methodology based on the "top down." In our approach the top-down method is paired with the optimization process for the automatic calculation of parameters of the various blocks constituting the system, and the size of these blocks. The optimization approach is based on multi objective genetic algorithms. This proposed methodology is used to find the optimal dimensional transistor parameters in order to obtain operational amplifier performances for analog and mixed CMOS-based circuit applications.**

Key-Words— Multi-objective Genetic Algorithm (MOGA), Optimization, CMOS Analog Circuit, Fully-Differential Folded Cascode Amplifier Operational.

I. INTRODUCTION

The evolution of the microelectronics industry is distinguished by the raising level of integration and complexity. It aims to decrease exponentially the minimum feature sizes used to design integrated circuits [1]. The cost of design is a great problem to the continuation of this evolution. Senior designer's knowledge and skills are required to ensure a good analogue integrated circuit design. To fulfil the given requirements, the designer must choose the suitable circuit architecture, although different tools partially automated the topology synthesis appeared in the past [2]-[6].

The use of efficient multiple-objective optimization algorithms is, therefore, of great importance to the automatic design of Op-Amp. Accuracy, ease of use, generality, robustness, and reasonable run-time are necessary for a circuit synthesis solution to gain acceptance by using optimization methods [7].

The approach uses a simulation based multi-objective optimization using a genetic algorithm to capture the optimal design points for a folded cascode OTA design. The method handles a wide variety of specifications and constraints, is extremely fast, and results in globally optimal designs. Our target was to design a folded cascode OTA circuit in sight of Pipeline analog-to-digital converter design using for wideband applications.

This paper is organized as follows. The folded cascode OTA structure is analyzed in section II. Section III presents the optimization approach proposed. Section IV gives the obtained results. Finally some concluding remarks are provided after evaluating our study toward other works.

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II. FULLY-DIFFERENTIAL FOLDED CASCODE AMPLIFIER

Fig.1 presents the Fully-Differential Folded Cascode (the name "folded cascode" comes from folding down p-channel cascode active loads of a diff-pair and changing the Mosfets to n-channels). This circuit is developed in part to improve the input common-mode range and power-supply rejection of the two stage op–amp. The "folded cascode" op-amp has a large gain and high bandwidth performances.

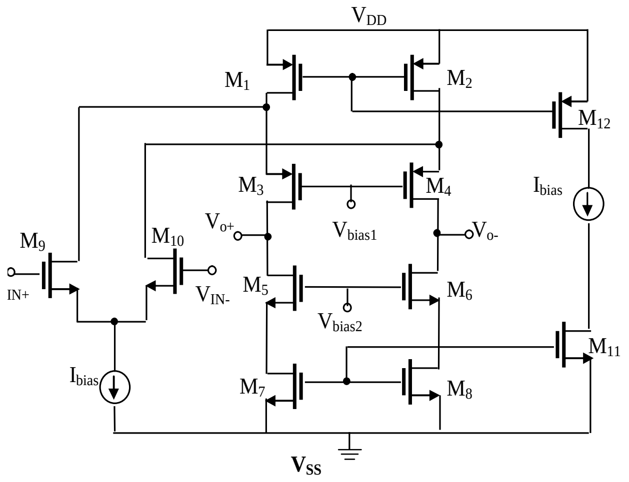

Fig.1. Fully-Differential Folded Cascode Amplifier

The unity gain bandwidth is given by the expression [1]:

$$GBW = \frac{g_{m9}}{C_L} \tag{1}$$

For the Folded Cascode, the open-loop voltage gain is given by [1]:

$$A_{V0} = \frac{g_{m9} \cdot g_{m6} \cdot g_{m4}}{I_D (g_{m4} . \lambda_N{}^2 + g_{m6} . \lambda_P{}^2)} \tag{2}$$

Where, gm4, gm6 and gm9 are respectively the transconductances of transistors M4, M6 and M9. ID is the bias current flowing in Mosfets M4, M6, and M9. CL is the capacitance at the output node, λ_n and λ_p are the parameters related to channel length modulation respectively for NMOS and PMOS devices.

For the Folded Cascode op-amp the slew rate is given by:

$$SR = \frac{I_{bias}}{C_L} \tag{3}$$

The formula of the power dissipated by the Op-amp is as follows [8]:

$$P = \left(V_{DD} - V_{SS}\right)(I_{bias} + 2I_1) \tag{4}$$

The area A of the Fully-Differential Folded Cascode op-amp is given by the sum of transistor and capacitor areas:

$$Area = \sum_{i=1}^{k} W_i L_i \tag{5}$$

III. Optimization approach

Optimal design of analog circuits is to find a set of variables x = {x_1, x_2, ..., x_n} that optimizes performance, such as gain, offset, signal to noise ratio, maximum operating frequency etc., while respecting the imposed specifications and / or constraints [9].

In the program, every individual is presented by a binary code string. From Fig. 1 we can see that there are 8 transistors and a biasing current to be adjusted. As a total there are 11 parameters to be adjusted and each gene of the chromosome stands for one parameter. Thus the parameter vector is compressed to [11]: [W_1, L_1, W_3, L_3, W_5, L_5, W_7, L_7, W_9, L_9, I_{bias}].

A weighted approach has been used to optimize op-amps. It uses adaptive weights along the optimization process to determine the overall fitness of an individual [10].

$$F = \sum_{i=1}^{n} \omega_i . f_i \tag{6}$$

Where ω_i is the weight coefficient of every sub-objective, f_i is the overall fitness of every performance considered and i is the number of the performance considered.

We used the MATLAB Optimization Toolbox to implement optimization by MOGAS. It starts by generating a random population of individuals. To pass from one generation k to generation k +1, the following operations are performed. At first, the population is reproduced by good selection where individuals reproduce better than bad. Then applied to a cross pairs of individuals (parents) of a certain proportion of the population (probability Pc, usually around 0.6) to produce new (children). A mutation operator is applied to a certain proportion of the population (probability P_m, the P_C generally much lower). Finally, the new individuals are evaluated and incorporated into the population of the next generation several stopping criteria of the algorithm are possible: the number of generations can be fixed a priori (time constant) or the algorithm can be stopped when the population does not evolve fast enough.

IV. Simulation Results

The proposed methodology will be applied folded-cascode op-amp (Fig. 1, table 1). In this simulation six performances are considered. They are the DC gain, bandwidth of unity-gain, phase margin, power, area, and Slew Rate. The optimization process optimizes the individual to improve its fitness score. This process will continue until the total number of generations is reached.

Performance measure	Spec	MOGA	Spectre	[6]	[1]
DC gain (dB)	≥70	84	70	70	75.57
Unity gain (MHz)	Max	1.56	1.06	50	19.14
Phase Margin (°)	≥ 60	70	88	60	67
Slew rate (V/µs)	Max	4.53	5.5	50	3.3
Area (µm2)	Min	140	140	720	/
Power (mW)	≤0.5	0.244	0.237	0.94	0.60
Technology (µm)		0.18	0.18	0.25	0.25

Table 1: Simulation results in MATLAB and Spectre and comparison with previous works

The results of the optimization scheme lead to a set of optimal solutions. The parameter values for the Folded Cascode topology of op-amp of the Pareto optimal designs, is indicated in table 1. In comparing for example the op-amp with the design presented in [1] and [6] the proposed approach op optimization has lead to better aspects (84dB gain, power consumption 250µW, 70° PM and 140 µm2 area).

V. CONCLUSION

This paper proposes an optimization approach based on Multi-Objective Genetic Algorithms, this approach enables the efficient and rapid generation of performance fronts of different topology of operational amplifiers. We demonstrated that by applying a multi-objective formulation, the design specifications of the circuit can be achieved by the MOGA optimization. The optimization procedure was implemented using the MATLAB optimization toolbox, and the circuit responses were obtained from Spectre. Experimental results for a folded-cascode, operational amplifiers show that this is a promising approach can be applied to optimize other basic analog IC blocks.

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