UNIVERSITÉ KASDI MERBAH DE OUARGLA

FACULTÉ DES NOUVELLES TECHNOLOGIES DE L'INFORMATION ET DE LA COMMUNICAT

DÉPARTEMENT D'ÉLECTRONIQUE ET DES TÉLÉCOMMUNICATIONS

FILIÈRE: ELECTRONIQUE

SPÉCIALITÉ: ELECTRONIQUE ET SYSTEM EMBARQUÉS

FPGA-based design and implementation of space vector modulation for three-phase three-level diode clamed inverter

Présenté Par: ***Mohamed CHELIGHEM, Abd Elhakim Yakoub CHAHED*** *Encadré par:* ***Mansour BOUZIDI***

Abstract

In inverter applications requiring medium to high power, the three-level diode clamped topology is a suitable way to achieve an enhanced quality of the output voltages and currents. This work presents an FPGA based implementation of space vector vector modulation for three-level diode clamped inverter. The three-level inverter using SVM control has superior performance though bringing about much computational complexity. Therefore, the XILINX Zynq 7000 FPGA-based implementation could solve this problem well.

Three-level diode clamped inverter

Multilevel inverters have opened the door for advances in electric energy conversion technology. They present the features of a lower device voltage rating, lower harmonic distortion, and higher efficiency compared with conventional two-level inverters.

Fig.1 shows a schematic diagram of a three-level diode-clamped inverter in which the DC-link consists of two capacitors C_1, C_2.

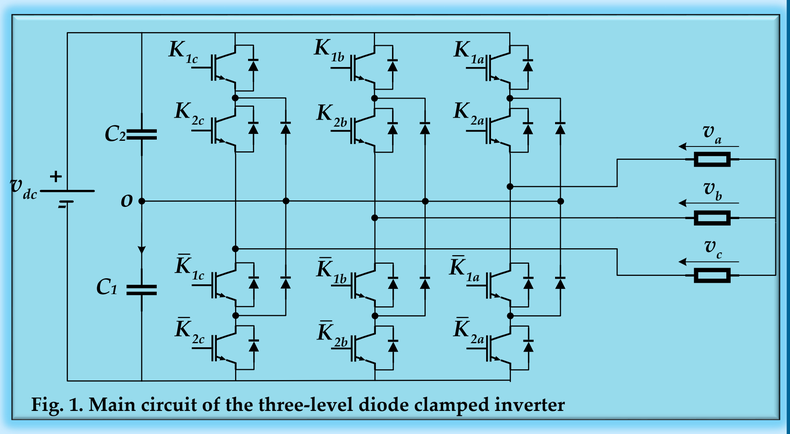


Fig. 1. Main circuit of the three-level diode clamped inverter

As showing in this table, each leg of the three-level inverter has three switching states (2, 1, 0), *x=a, b or c.*

Switching states	K_{2x}	K_{1x}	v_{xo}
2	1	1	$v_{dc}/2$
1	0	1	0
0	0	0	$-v_{dc}/2$

The expressions of instantaneous inverter phase output voltages are given by:

$$v_a = (2v_{ao} - v_{bo} - v_{co})/3$$
$$v_b = (-v_{ao} + 2v_{bo} - v_{co})/3$$
$$v_c = (-v_{ao} - v_{bo} + 2v_{co})/3$$

The coordinates of each switching vector v_α, v_β are calculated based on the following matrix transformation:

$$\begin{bmatrix} v_\alpha \\ v_\beta \end{bmatrix} = \sqrt{\frac{2}{3}} \begin{bmatrix} 1 & -1/2 & -1/2 \\ 0 & \frac{\sqrt{3}}{2} & -\frac{\sqrt{3}}{2} \end{bmatrix} \begin{bmatrix} v_a \\ v_b \\ v_c \end{bmatrix}$$

Using the different switching combinations, the three-level inverter has 27 switching vectors, these vectors can be described using a graphical representation in three-dimensional space as shown in Fig. 2.

The diagram of space vectors can be divided into six sectors, each sector further is divided into four traiangle.

Space vector modulation of three-level inverter

The control of the multilevel inverters can be achieved by several modulation techniques, among them, the space vector modulation (SVM) stands out, since it offers significant flexibility to optimize switching waveforms.
SVM is a discrete type of modulation technique in which a sampled reference vector v^*, is synthesized by the time average of a number of appropriate switching state vectors.

The three-level SVM algorithm has three-main steps as shown in Fig. 3.

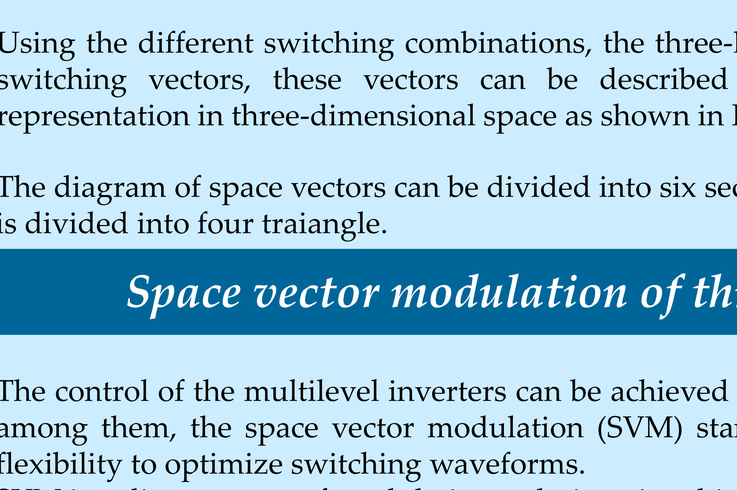


Fig. 2. Space voltage vectors for a three-level inverter

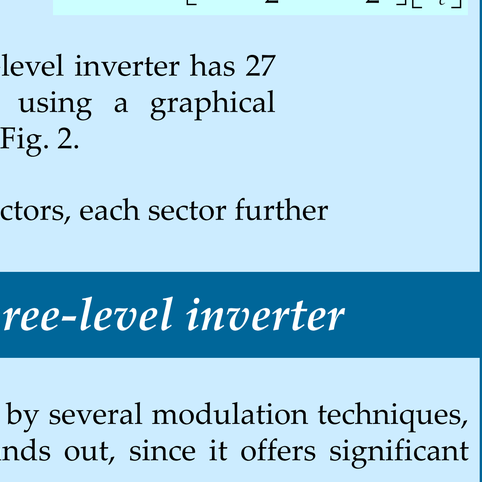


Fig. 3. Three-level space vector modulation algorithm

Field-Programmable Gate Arrays FPGA

The FPGA is a integrated circuit configured with a hardware description language. Its unique design allows custom design of the hardware. From a high-level view the FPGA is a programmable silicon chip. It uses logic blocks and programmable routing resources, realizing this tailored version, without physically changing anything in the hardware (see Fig. 4).

Fig. 4: Different parts of the FPGA

The digital computing tasks are developed in the software (ie general-purpose and graphical programming languages) and then compiled down to a configuration file or bitstream, containing information on how the components should be wired together. The FPGA does not require the user to have experience in hardware-design, which broadens the user group (see Fig. 5).

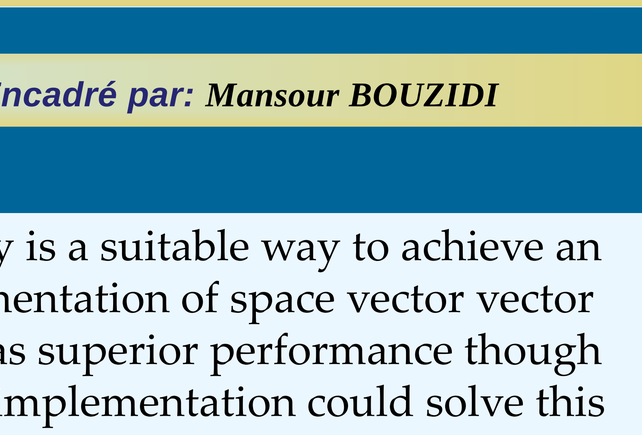
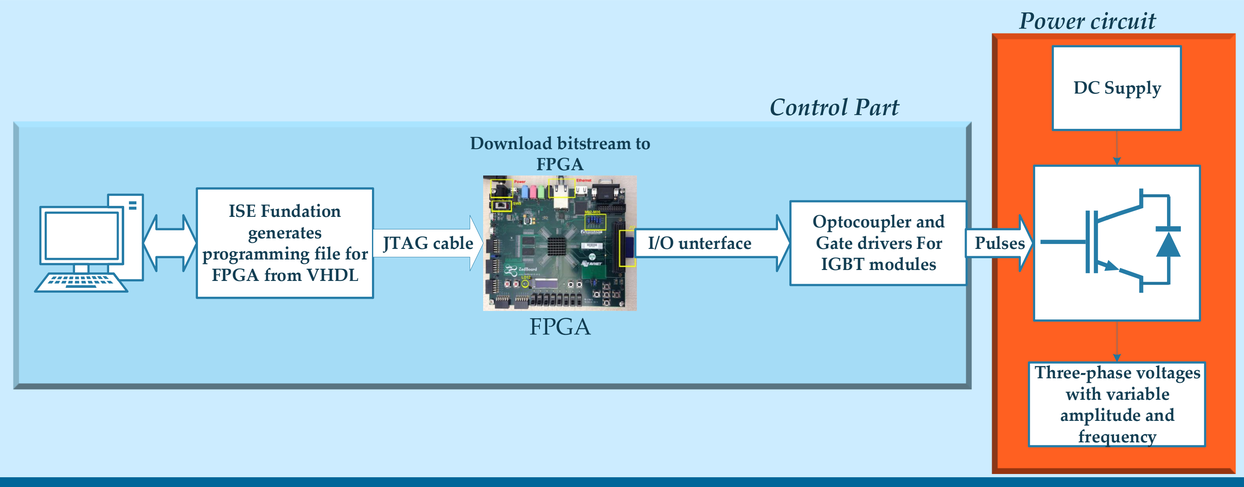
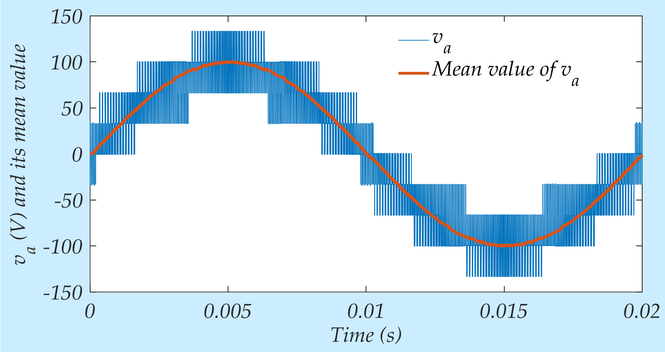


Fig. 5: XILINX FPGA design flow

Design and control of three-level inverter based on FPGA



Simulation results



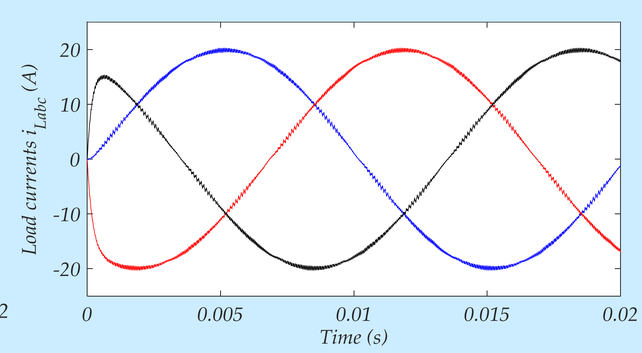


Fig.6. Output phase voltage and load currents of three-level inverter controlled by SVM

Conclusion

In this work, SVM for three-level inverter is implemented using FPGA. The SVM algorithm is verified by modeling the simulation system in Matlab/ Simulink.
The FPGA may provide multiple PWM generators according to the three-level inverter requirements. Unlike the digital signal processor (DSP) which runs a sequential program in its microprocessor, an FPGA may run all the operations in parallel with the clock signal.
The remaining task of this work is to complement the control and power circuits to extract the experimental results.

REFERENCES

Thesis, papers, and docs at Xilinx website