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Design and implementation of three-dimensional space vector modulation for three phase four-leg inverter based on FPGA

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Abstract

The four-leg inverter has been shown to be a solution for inverters operating in four-wire distribution systems. The technique three-dimensional space vector modulation (3DSVM) used is a reliable solution as it utilizes DC bus voltage more efficiently. The objective of this work is to design a controller circuit of 3DSVM for a three phase four-leg inverter. The implementation is done on Zynq 7000 FPGA board using hardware description language (VHDL). FPGA provides a very attractive high-level design/simulation tool called as Xilinx ISE; it is a very flexible tool, which allows testing of a high-level structural description of the design and make possibilities for quick changes and corrections in the design.

Three-phase four-leg inverter

In several areas, power is distributed through three-phase four-wire system and traditional three-phase three-wire inverters are inadequate for various applications. The most popular topologies are two-level voltage source inverter (VSI) based, namely, split capacitor, three H-bridge, and four-leg. This later has been shown to be a solution for inverters operating in four-wire systems and it offers full utilization of the DC-link voltage and lower stress on the DC-link capacitors.

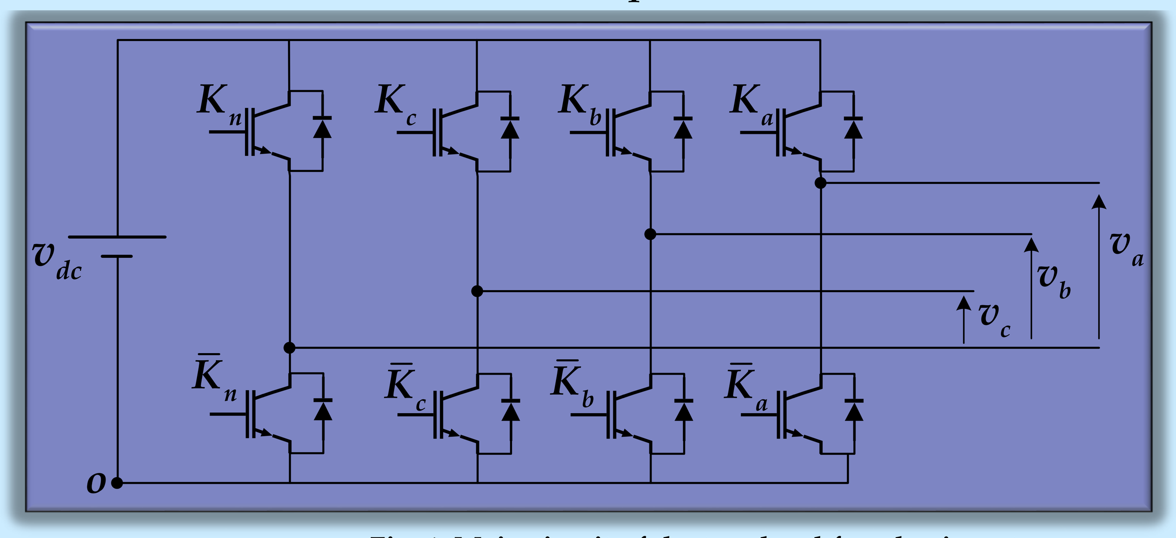


Fig. 1. Main circuit of the two-level four-leg inverter

The instantaneous output inverter phase to neutral voltages v_a, v_b and v_c are given as:

$$\begin{bmatrix} v_a \\ v_b \\ v_c \end{bmatrix} = v_{dc} \begin{bmatrix} K_a - K_n \\ K_b - K_n \\ K_c - K_n \end{bmatrix}$$

Because each leg has two switching stats, there are 16 possible switch combinations.

The 16 switching vectors can be sorted into five layers.

The diagram of space vectors can be divided into six sectors with every sector further formed by 4 tetrahedrons (see Fig. 2).

Three-dimensional Space vector modulation of four-leg inverter (3DSVM)

The traditional two dimensional SVM algorithms only can be used to control converter connected to power system with balanced voltage/current where the homopolar component in Concordia transformation is equal to zero. In the four-wire system distribution, the case of unbalanced voltage is taken in consideration; therefore, the homopolar component is not equal to zero. Thus, three dimensional space vector modulation (3DSVM) algorithms must be taken into account in order to generate the desired signal.

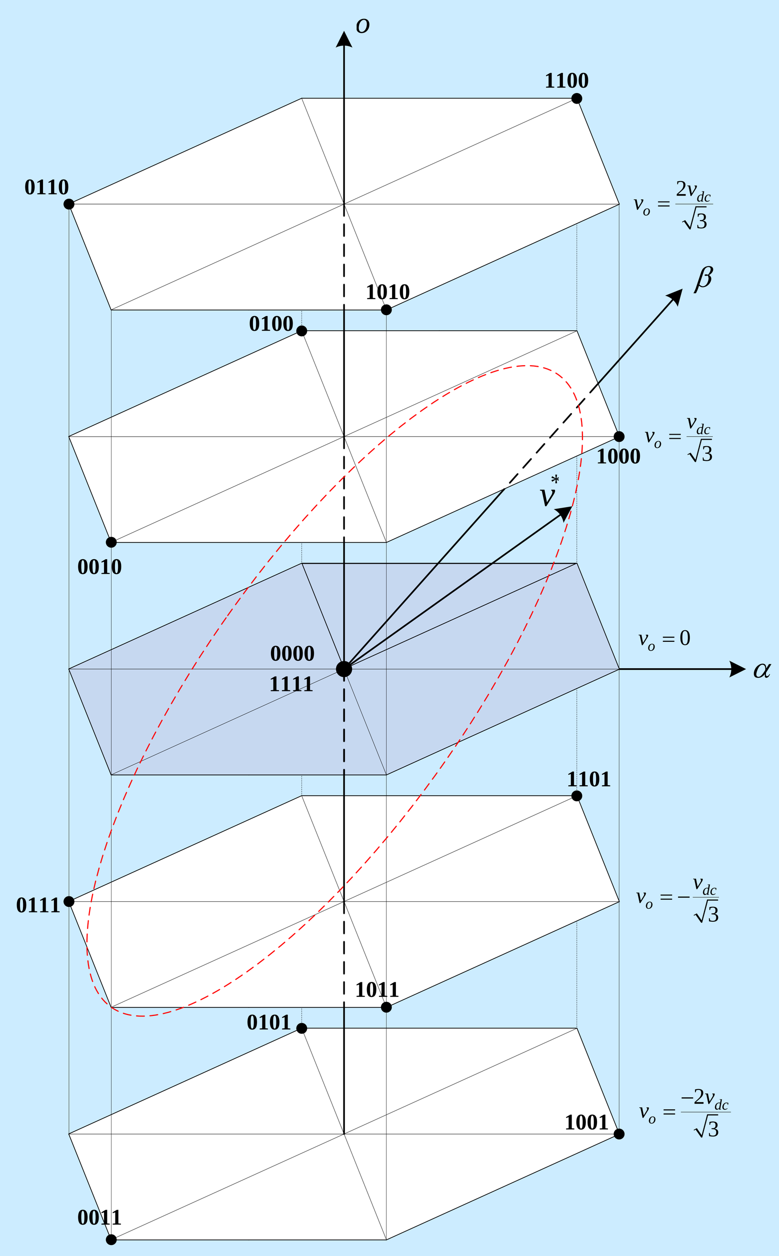


Fig. 2. Space voltage vectors for a four-leg inverter

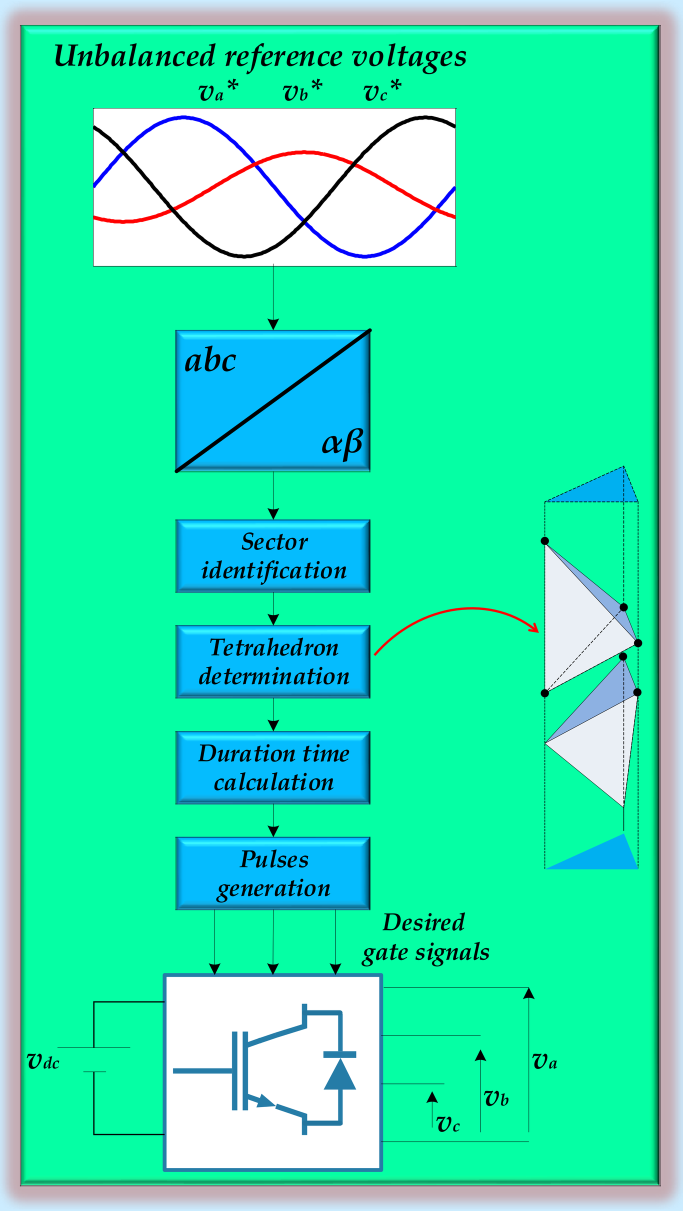


Fig. 3. Three-dimensional space vector modulation algorithm

Field-Programmable Gate Arrays FPGA

Field Programmable Gate Arrays (FPGAs) are semiconductor devices that are based around a matrix of configurable logic blocks (CLBs) connected via programmable interconnects. FPGAs can be reprogrammed to desired application or functionality requirements after manufacturing. This feature distinguishes FPGAs from Application Specific Integrated Circuits (ASICs), which are custom manufactured for specific design tasks.

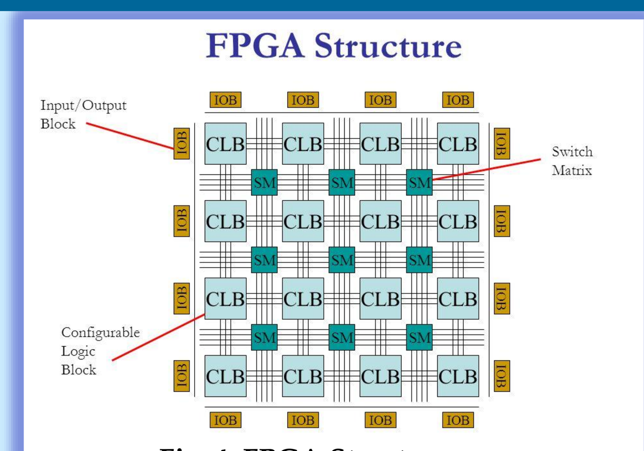


Fig. 4: FPGA Structure

The digital computing tasks are developed in the software (ie general-purpose and graphical programming languages) and then compiled down to a configuration file or bitstream, containing information on how the components should be wired together. The FPGA does not require the user to have experience in hardware-design, which broadens the user group (see Fig.5).

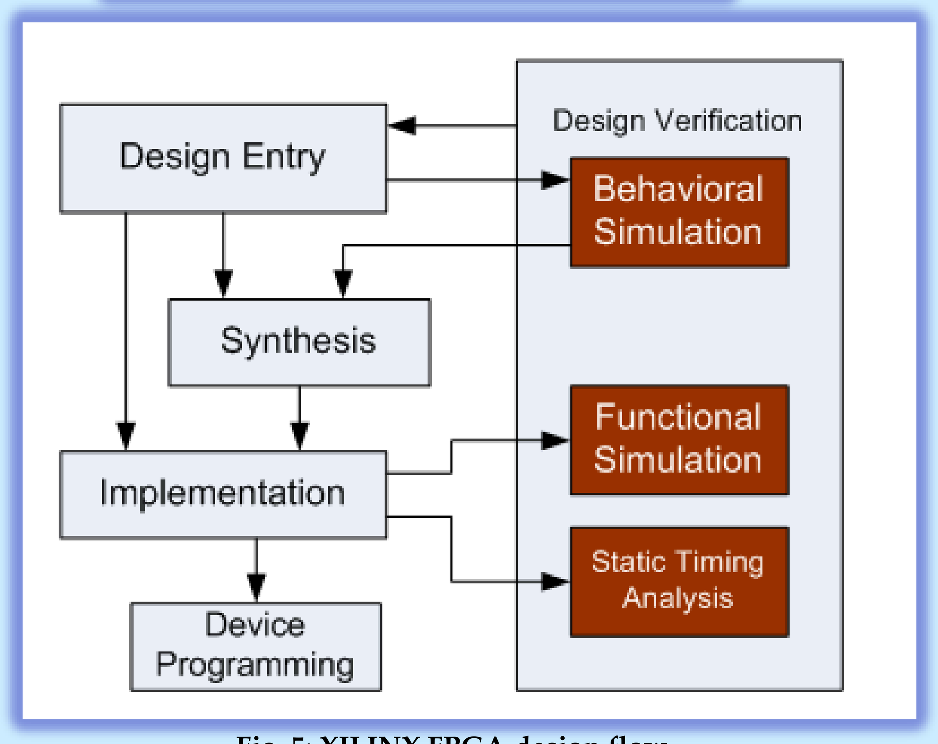
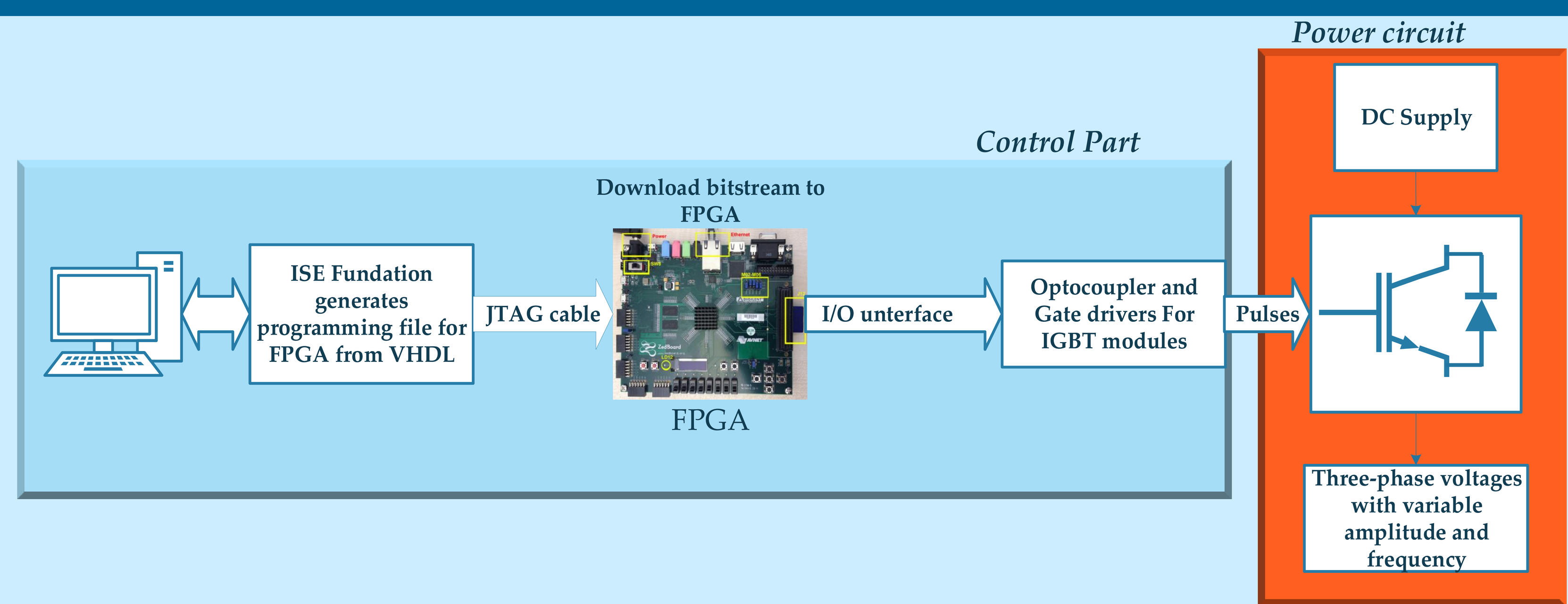


Fig. 5: XILINX FPGA design flow

Design and control of four-leg inverter based on FPGA



Simulation results

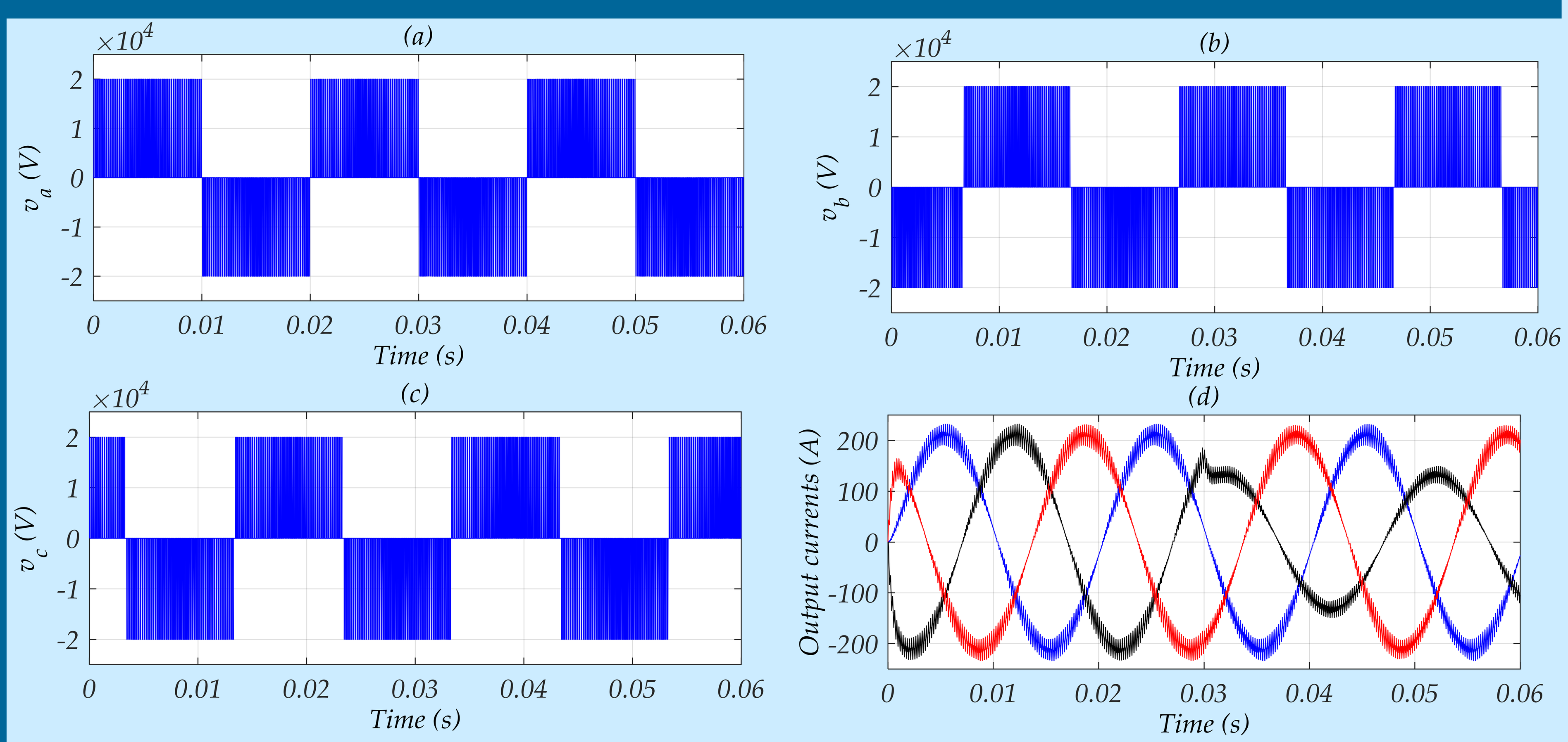


Fig. 6: output voltages and currents of four-leg inverter controlled by 3DSVM

Conclusion

This work analysis and implement a three-dimensional space vector modulation algorithm for three-phase four-leg inverter based on FPGA. The FPGA may be the natural choice because of its high-speed operation and capacity to handle multiple PWM signals.

The remaining task of this work is to complement the control and power circuits to extract the experimental results.

REFERENCES

Thesis, papers, and docs at Xilinx website