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THEME

Design and implementation of three-dimensional space vector modulation for three-phase four-leg inverter based on FPGA

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Contents

List of Abbreviations

SVM (Space vector Modulation)

PWM (Pulse Width Modulation)

SPWM (Sinusoidal pulse width Modulation)

2-DSVM (Two Dimensional Space Vector Modulation)

3-D SVM (Three Dimensional Space Vector Modulation)

SAPF (Shunt Active Power Filter)

HBCC (Hysteresis Band Current Control)

DC (Direct Current)

AC (alternating current)

THD (total harmonic distortion)

VHDL (VHSIC Hardware Description language)

FPGA (field programmable gate arrays)

CLB (configurable logic block)

IOB (input/output block)

LUT (lookup table)

DCM (Digital Clock Manager)

DDR (Double Data Rate)

ISE (Integrated Synthesis Environment)

XST (Xilinx Synthesis Technology)

NGD (Negative Generic Database)

NGC (Negative Generic Circuit)

UCF (User Constraints File)

NCD (Negative Circuit Description)

DSP (digital signal processors)

CPU (Central Processing Unit)

RAM (Random-access Memory)

SRAM (Several RAM)

ROM (Read-Only Memory)

EPROM (Erasable Programmable Read-Only Memory)

IGBT (Insulated-Gate Bipolar Transistor)

RTL (Register Transfer Level)

List of Symbols

v	Output Voltage Vector
v_{dc}	DC source voltage
α	Real axis
β	Imaginary axis
γ	Third dimensional axis
v_{ao}, v_{bo}, v_{co}	Outputs inverter phase voltages
v^*	Reference voltage vector
V_m	Amplitude
T_s	Switching period
t_i	Duration time
$v_\alpha^*, v_\beta^*, v_\gamma^*$	Coordinates of the reference voltage vector
$S_x, x = a,b,c,n$	Switching functions
$v_{ao}, v_{bo}, v_{co}, v_{no}$	Neutral
W	Angular frequency
v_1, v_2, v_3, v_4	Switching vectors

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General introduction

In recent years, the four-leg topology for three-phase with neutral inverters have been used in many applications, such as controlled rectifiers[1],[2], active power filters [2], [3], and, in general, in applications that require a precise neutral current control. This topology presents the advantage of adding an extra degree of freedom, expanding the control capabilities of the inverter using the same DC-link capacitors and voltages compared with the other classic topology that uses a split capacitor inverter with three legs [1].

Several modulation methods for four-leg converter have been suggested [1], [2], [4], [5].A space vector modulation (SVM) control is deemed advantageous over a carrier based pulse width modulation (PWM) because it has a higher DC bus utilization, less output voltage/current harmonics, less switching loss and is suitable for implementation using a digital controller. For a traditional three-legged power converter, where a balanced case or absence of the zero sequence is always assumed, a space vector is defined in a two-dimensional (2D) plane and a SVM is performed in the two-dimensional plane (2DSVM). For the four-legged power converters, the SVM must be performed in three-dimensional space (3DSVM), which make it more complex than conventional SVM in two-dimensional space [1], [2], [4], [5].

In other side, the digital signal processors (DSP) and microcontrollers are widely used power electronics PWM controls due to their advantages, such as software flexibility, mature application, satisfying performance and low cost [6], [7]. However, it also suffers some disadvantages: 1) As a sequence controller, these type processors interpret instructions line by line, which results in time delay and leads to deteriorate the performance of a control system. 2) With most computation resources devoting to the periodic events such as sampling, control algorithm calculating and PWM gating signals generating, limited resources are left to other functions [7].

Alternatively, the advanced field programmable gate array (FPGA) may provide multiple PWM gate signals according to the system requirements [7]. Since FPGA can carry out parallel processing by means of hardware mode, which occupies nothing of the CPU, a very high speed level of the system can be obtained as well as an exciting precision [7]. Therefore, the FPGA-based switching control technology could be the first choice for power electronics converters [7].

The main objective of this thesis is to design a switching controller based on three-dimensional space vector modulation for a three-phase four-leg inverter. The 3DSVM used is a reliable solution as it utilizes DC bus voltage more efficiently. The Xilinx ZedBoard Zynq-7000 development board is used to implement 3DSVM for four-leg inverter. The VHDL-code-based behavioral models of different 3DSVM blocks are designed and synthesized using the Project Navigator tool of the Xilinx ISE Design Suite 14.7 software.

This memoir is divided into three chapters, which are summarized as follows:

The operating principle and mathematical modeling of three-phase four-leg inverter are presented in chapter one.

In chapter two, the three-dimensional space vector modulation algorithm for two-level four-leg inverter is presented and analyzed in detail.

The third chapter is devoted to the implementation of the three-dimensional space vector modulation for four-leg inverter based on FPGA.

Finally, a main conclusion and some future works are given.

Chapter I:

Modeling and analysis of three-phase four-leg inverter

I.1. Introduction

In three-phase four-wire systems and unbalanced mode, the four-leg inverters have been considered as one of the adapted topologies of the power converters for the application which require a very strict and precise control of the neutral current, caused by the unbalanced and/or nonlinear load or unbalanced source.

This chapter presents the operating principle and mathematical modeling of three-phase four-leg inverter.

I.2. Four-wire three-phase inverter topologies

Three-phase voltage-source inverters normally have two ways of providing a neutral connection for three-phase four-wire systems:

1- Using split dc link capacitors and tying the neutral point to the mid-point of the dc link capacitors;
2- Using a four-leg converter topology and tying the neutral point to the mid-point of the fourth neutral leg.

I.2.1. Three-phase four-wire inverter with split dc-link capacitors

As shown in figure (I. 1), the three-phase four-wire inverter with split dc-link capacitors utilizes the standard three-phase conventional inverter where the DC capacitor is split and the neutral wire is directly connected to the electrical midpoint of the capacitors [8]. The split capacitors allow load neutral current to flow through one of the DC capacitors, and return to the AC neutral wire.

One of the serious problems with this topology is voltage unbalance between the capacitors [9]. This is due to the direct flow of the neutral current through one of the capacitors, causing voltage variations among them.

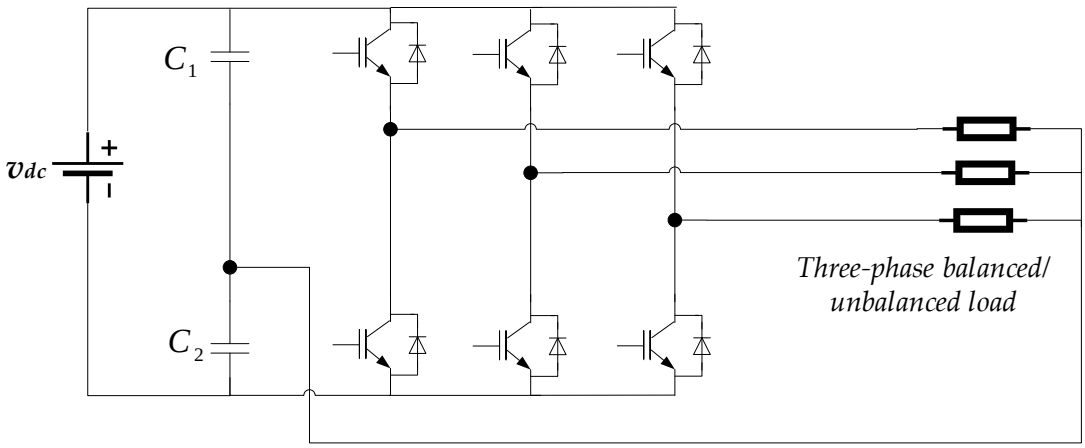


Figure (I.1): Three-phase split dc-link capacitors inverter topology

I.2.2. Three-phase four-leg topology

Figure (I.2) shows the four-leg inverter topology used in three-phase four-wire systems [9]. In this topology, three of the switch legs are connected to the three-phase load while the fourth switch leg is connected directly to the neutral point of the load. This topology is most suitable for compensation of high neutral currents [10]. Despite having, higher number of switching devices this topology outweighed the split-capacitor topology by number of factors [9].

- Better controllability: In this topology, only one DC-bus voltage needs to be regulated, as opposed to two in the capacitor midpoint topology. This significantly simplifies the control circuitry with better controllability.
- Lower DC voltage and current requirement.

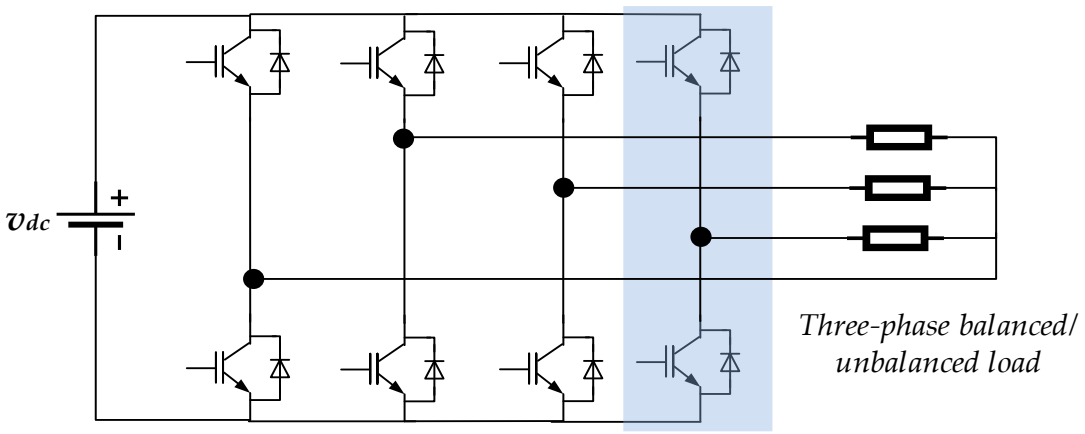


Figure (I.2): Three-phase four-leg inverter topology

The comparison of three-phase four-wire SAPFs are given in table (I. 1) [9]. The significant factor that may decide the selection of these topologies is the overall cost involved to realize the three-phase four-wire SAPF. For better performance at moderate cost, the four-leg topology could be a best option for low-to-medium-power applications [9].

Table (I.1): Comparison between three-phase four-wire inverter topologies [9]

SAPF topologies	***Capacitor midpoint***		***Four-leg***
Number of switching devices (2-level inverter)	6		8
Number of capacitors	2		1
Additional sensor requirement	One extra DC bus voltage sensor (total two)		One extra current sensor
Control over neutral current	Indirect		Direct (using 4th leg)
Effectiveness of neutral current compensation	May degrade with high neutral currents		Better performance than capacitor midpoint
Overall cost	Low		Moderate
Main advantage	Least number of switching devices		Better controllability
Main disadvantage	Capacitor unbalance problem due to voltage difference across two capacitors		More number of switching devices
Application and topology selection	Suitable for low to medium power applications		Suitable for low to medium power applications. Suitable for compensating high neutral currents

There is a growing interest in four-leg converters for three-phase four-wire applications. Some of the typical applications are as follow

1- Distributed power generators, such as micro-turbine generators and fuel cell based generators, which may run in either stand-alone or grid parallel mode. These distributed power generators adopt four-leg inverters to provide a three-phase output with a neutral connection.

2- Active power filters, where four-leg converters are proposed for compensating the harmonic current through the neutral point.

3- Three-phase PWM rectifiers, where the additional fourth leg provides flexibility to deal with the line distortion and imbalance, as well as fault tolerant capability.

I.3. Modeling of three-phase four-leg inverter

Figure (I. 3) shows a typical four-leg inverter structure. An additional wire connects the load side neutral to the midpoint of the fourth leg. The inverter is composed of eight IGBT transistors with a freewheeling diode in parallel with each active switch to ensure bidirectional flow of the output current. Each leg of the three-phase four-leg inverter has upper and lower switches. The lower switches of the four legs are complementary to the upper switches in order to avoid short-circuiting the DC source.

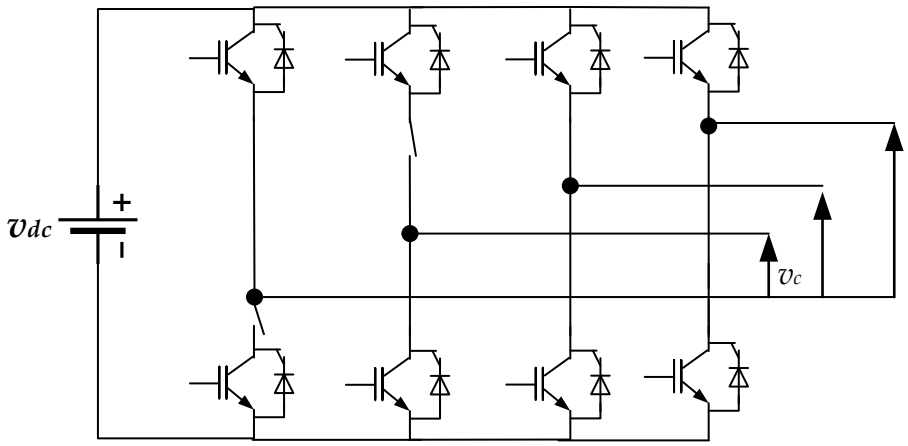


Figure (I.3): Power circuit of three-phase four-leg inverter

To describe the operation of the four-leg inverter, a switching function can be defined as:

$$S_x = \begin{cases} 1, \text{ if } K_x \text{ is on} \\ 0, \text{ if } K_x \text{ is off} \end{cases}, \quad x = a,\ b,\ c \text{ or } n \tag{I.1}$$

Considering voltage of node "*o*" as the reference voltage, the voltage v_{xo} can be expressed as:

$$v_{xo} = S_x v_{dc} \tag{I.2}$$

The instantaneous output inverter phase to neutral voltages v_a, v_b and v_c can be expressed as:

$$\begin{bmatrix} v_a \\ v_b \\ v_c \end{bmatrix} = \begin{bmatrix} v_{a0} - v_{n0} \\ v_{b0} - v_{n0} \\ v_{c0} - v_{n0} \end{bmatrix} \tag{I.3}$$

It can be expressed in terms of switching functions and DC-link voltage as given by:

$$\begin{bmatrix} v_a \\ v_b \\ v_c \end{bmatrix} = v_{dc} \begin{bmatrix} S_a - S_n \\ S_b - S_n \\ S_c - S_n \end{bmatrix} \tag{I.4}$$

I.3.1 Switching vectors in the Three-Dimensional Space ($\alpha\beta\gamma$)

The coordinates of each switching vector, v_α, v_β and v_γ are calculated by:

$$\begin{bmatrix} v_\alpha \\ v_\beta \\ v_\gamma \end{bmatrix} = \sqrt{\frac{2}{3}} \begin{bmatrix} 1 & -1/2 & -1/2 \\ 0 & \frac{\sqrt{3}}{2} & -\frac{\sqrt{3}}{2} \\ \frac{1}{\sqrt{2}} & \frac{1}{\sqrt{2}} & \frac{1}{\sqrt{2}} \end{bmatrix} \begin{bmatrix} v_a \\ v_b \\ v_c \end{bmatrix} \tag{I.5}$$

Because each leg has two switching stats, there are sixteen possible switch combinations. The switching combinations can be represented by the ordered sets (S_a S_b S_c S_n), Figure (I. 4) shows all these sixteen switching combinations.

By applying (I .5) for different switching combinations, the output voltages in abc and $\alpha\beta\gamma$ coordinates all sixteen switching combinations are listed in table (I.2).

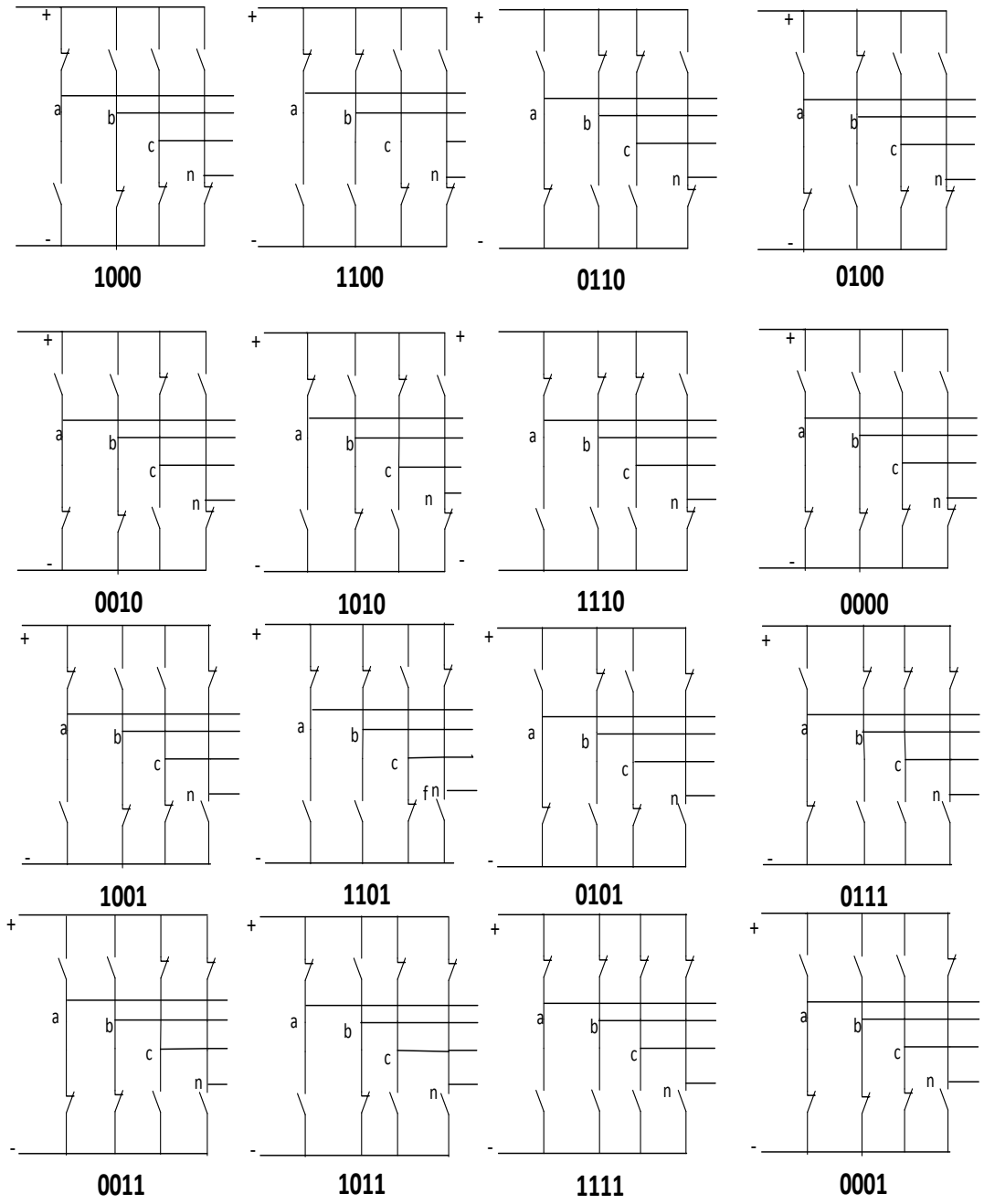


Figure (I.4) Sixteen possible switching combination

Switching states	v_{an}	v_{bn}	v_{cn}	v_{α}	v_{β}	v_{γ}
1000	v_{dc}	0	0	$\sqrt{\frac{2}{3}}v_{dc}$	0	$\frac{v_{dc}}{\sqrt{3}}$
1001	0	$-v_{dc}$	$-v_{dc}$	$\sqrt{\frac{2}{3}}v_{dc}$	0	$\frac{-2v_{dc}}{\sqrt{3}}$
1100	v_{dc}	v_{dc}	0	$\frac{v_{dc}}{\sqrt{6}}$	$\frac{v_{dc}}{\sqrt{2}}$	$\frac{2v_{dc}}{\sqrt{3}}$
1101	0	0	$-v_{dc}$	$\frac{v_{dc}}{\sqrt{6}}$	$\frac{v_{dc}}{\sqrt{2}}$	$\frac{-v_{dc}}{\sqrt{3}}$
0100	0	v_{dc}	0	$\frac{-v_{dc}}{\sqrt{6}}$	$\frac{v_{dc}}{\sqrt{2}}$	$\frac{v_{dc}}{\sqrt{3}}$
0101	$-v_{dc}$	0	$-v_{dc}$	$\frac{-v_{dc}}{\sqrt{6}}$	$\frac{v_{dc}}{\sqrt{2}}$	$\frac{-2v_{dc}}{\sqrt{3}}$
0110	0	v_{dc}	v_{dc}	$\sqrt{\frac{2}{3}}v_{dc}$	0	$\frac{2v_{dc}}{\sqrt{3}}$
0111	$-v_{dc}$	0	0	$\sqrt{\frac{2}{3}}v_{dc}$	0	$\frac{-v_{dc}}{\sqrt{3}}$
0010	0	0	v_{dc}	$\frac{-v_{dc}}{\sqrt{6}}$	$\frac{-v_{dc}}{\sqrt{2}}$	$\frac{v_{dc}}{\sqrt{3}}$
0011	$-v_{dc}$	$-v_{dc}$	0	$\frac{-v_{dc}}{\sqrt{6}}$	$\frac{-v_{dc}}{\sqrt{2}}$	$\frac{-2v_{dc}}{\sqrt{3}}$
1010	v_{dc}	0	v_{dc}	$\frac{v_{dc}}{\sqrt{6}}$	$\frac{-v_{dc}}{\sqrt{2}}$	$\frac{2v_{dc}}{\sqrt{3}}$
1011	0	$-v_{dc}$	0	$\frac{v_{dc}}{\sqrt{6}}$	$\frac{-v_{dc}}{\sqrt{2}}$	$\frac{-v_{dc}}{\sqrt{3}}$
1110	v_{dc}	v_{dc}	v_{dc}	0	0	$\sqrt{3}v_{dc}$
1111	0	0	0	0	0	0
0000	0	0	0	0	0	0
0001	$-v_{dc}$	$-v_{dc}$	$-v_{dc}$	0	0	$-\sqrt{3}v_{dc}$

Table (I.2): Output voltages in abc and $\alpha\beta\gamma$ coordinates for all sixteen switching states

The distribution of the sixteen switching vectors expressed in table (I. 2) are represented graphically in figure (I. 5). There are two zero switching vectors (1111, 0000), and fourteen non-zero switching vectors. It can be viewed as that each of the switching vector for a three-leg inverter splits into two switching vectors, depending on switch position of the neutral leg. All the sixteen switching vectors can be sorted into several layers. The two zero vectors, 1111 and 0000, locate at the origin of the $\alpha\beta\gamma$ coordinate. On the layer of $\frac{v_{dc}}{\sqrt{3}}$, there are three switching vectors, 1000, 0100 and 0010. On the layer of $\frac{2v_{dc}}{\sqrt{3}}$, there are three switching vectors, 1100, 0110 and 1010. On the layer of $\sqrt{3}v_{dc}$, there is only one switching vector 1110. On the layer of $-\frac{v_{dc}}{\sqrt{3}}$, there are three switching vectors, 1011, 1101 and 0111. On the layer of $-\frac{2v_{dc}}{\sqrt{3}}$, there are three switching vectors, 1001, 0101 and 0011. On the layer of $-\sqrt{3}v_{dc}$, there is only one switching vector 0001.

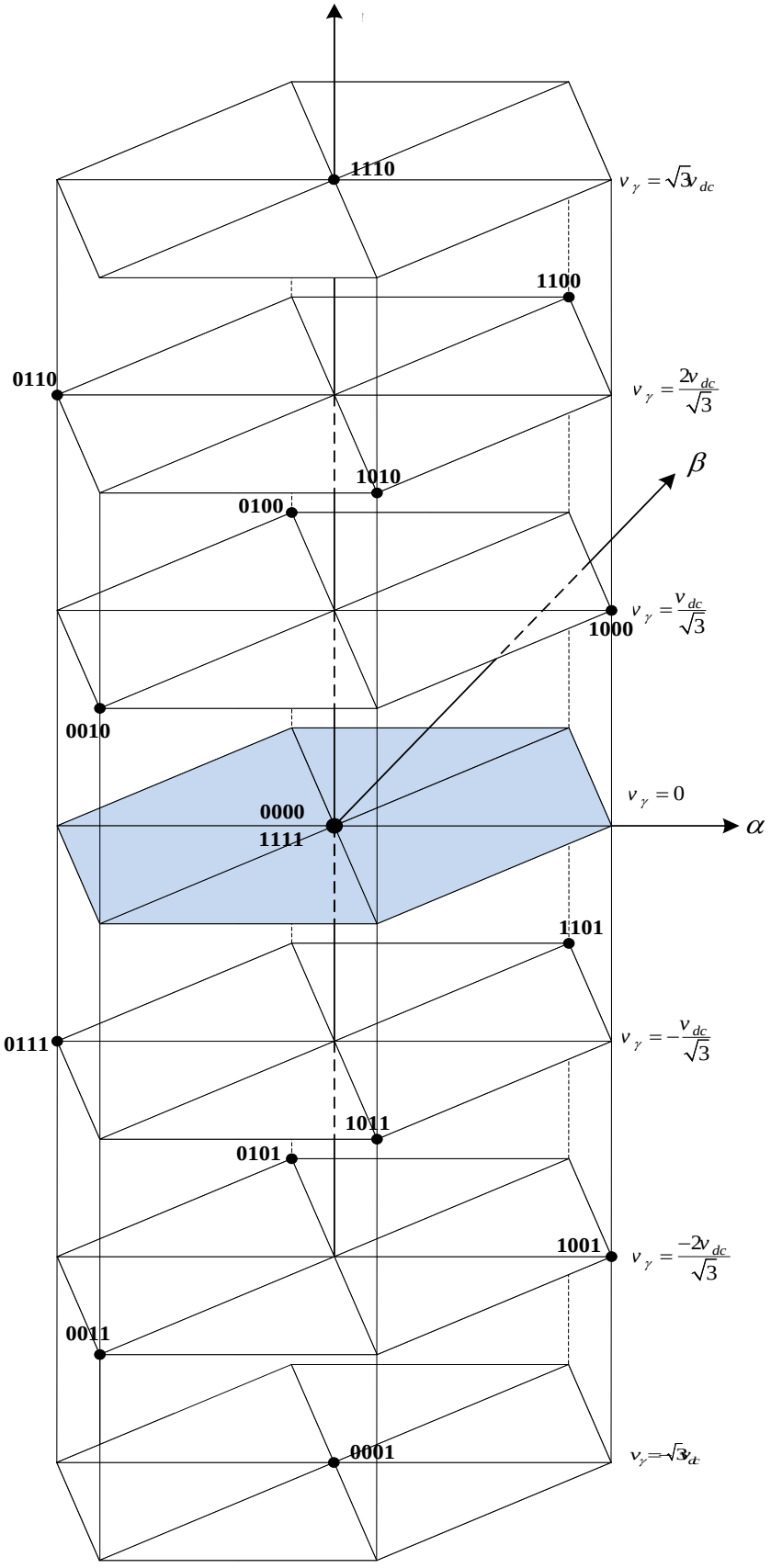


Figure (I. 5) Switching vectors in $\alpha\beta\gamma$ space

As shown in figure (I. 6), the diagram of space vectors can be divided into six prisms, each prism further is divided into four tetrahedrons.

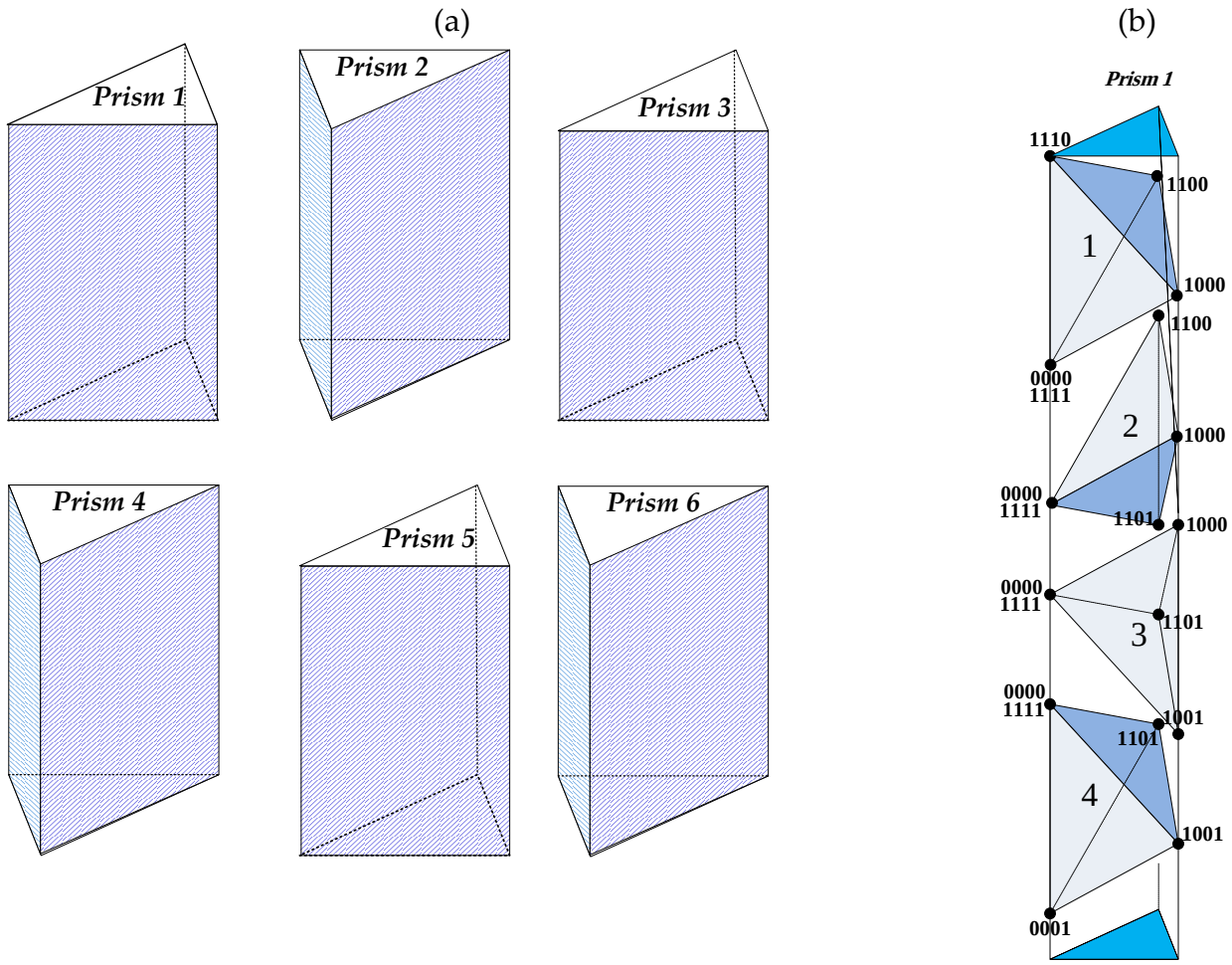


Figure (I. 6): (a) Three-dimensional prisms, (b): Tetrahedrons in the first prism

I.4. Conclusion

This chapter was mainly devoted to the analysis and modeling of three-phase four-leg inverter, the output voltages in terms of switching states and DC-link voltage are given. According to the number switching states, the four-leg inverter can provide sixteen switching voltages; these switching voltages are represented in three-dimensional space $\alpha\beta\gamma$.

The next chapter will be devoted to the application of three-dimensional space vector modulation to control the three-phase four-leg inverter.

Chapter II:

Three-dimensional space vector modulation of three-phase four-leg inverter

II.1. Introduction

The converter switching must be controlled to follow a control reference and modulation strategies are in charge to define the switching control in the converter. The primary objective of the modulation algorithm is to synthesize a control reference obtaining a pulse train with the same averaged value. Several modulation strategies have been proposed in the literature to control the voltage source inverter, among them, hysteresis band current control (HBCC) [11], carrier based PWM [12], and space vector modulation (SVM) [13]. Space vector modulator may be the most favorable and popular

modulation scheme for most three-phase applications because it can render lower output voltage/current distortion than other modulation techniques, especially at high modulation index range [14]. In addition, the switching losses and harmonic spectrum can be minimized.

Indeed, the two dimensional SVM algorithms cannot be used to control a four-leg inverter [14]. Therefore, prior art of SVM for four-leg inverters is formulated in a three-dimension space (3DSVM).

The objective of this chapter is to present the three-dimensional space vector modulation (3DSVM) for two level four-leg inverter.

II.2. Three Dimensional Space Vector Modulation

A 3DSVM is a discrete type of modulation technique in which a voltage reference vector v^* is synthesized by the time average of a number of appropriate switching state vectors [15].

II.2.1. Reference voltage vector in $\alpha\beta\gamma$ space

The reference voltages are generally three-phase balanced or unbalanced voltages given as follow:

$$\begin{aligned} v_a^* &= V_{m1}\sin\omega t \\ v_b^* &= V_{m2}\sin\left(\omega t - \frac{2\pi}{3}\right) \\ v_c^* &= V_{m3}\sin\left(\omega t - \frac{4\pi}{3}\right) \end{aligned} \tag{II.1}$$

Where: $\omega = 2\pi f$ is the angular frequency.

The reference voltages in $\alpha\beta\gamma$ coordinate is calculated using (I.5):

Projection of three-phase reference voltages into the $\alpha\beta o$ plane is a vector called the reference voltage vector $v^* = \begin{bmatrix} v_\alpha^* & v_\beta^* & v_\gamma^* \end{bmatrix}^T$, it rotates counterclockwise in space diagram with angular frequency of ω as shown in figure (II.1).

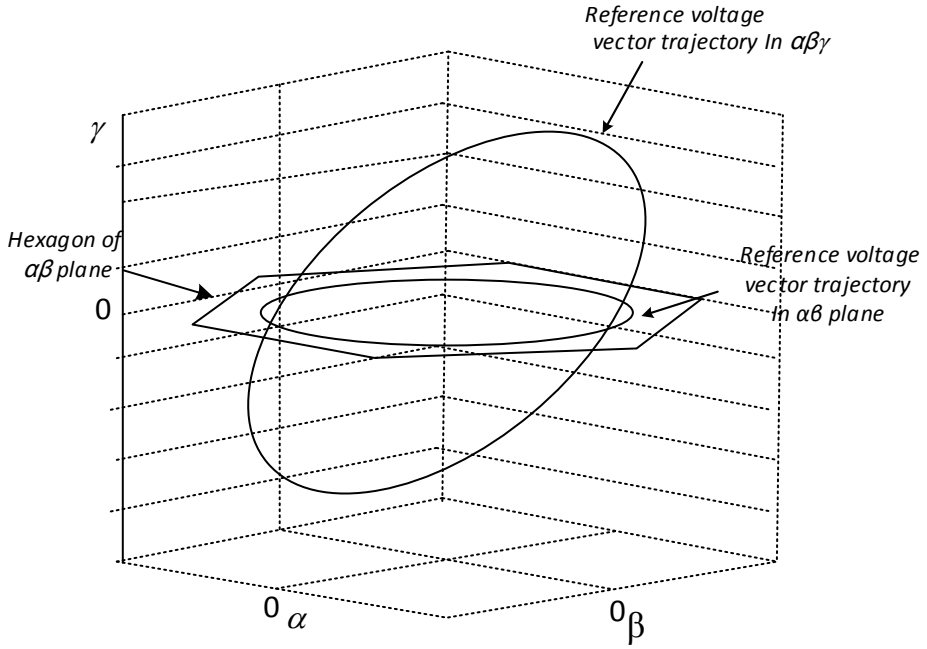


Figure (II.1): Balanced and unbalanced reference voltage vector representation in $\alpha\beta$ plane and $\alpha\beta\gamma$ space.

II.2.2. 3DSVM algorithm

When the reference voltage vector is located in a known prism at any sampling instant, the tip of the voltage vector lies in a tetrahedron formed by the four switching vectors adjacent to it. These adjacent switching vectors are used to synthesize the reference voltage vector [15].

The synthesis of the reference voltage vector takes the following three steps [14]:

1- Determination of the space vector location;

2- Duration time calculation;

3- Pulses generation.

II.2.2.1. Determination of the space vector location

The space vector location is determined in two steps: (1) determining the prism number of where the vector lies, and (2) determining the tetrahedron number of where the reference vector is located [14].

Step 1: Prism number computation

Six prisms must be identified. They are numbered as prism 1 to prism 6 (see Figure (I.6). The determination of the prism is similar to the selection of sector in the 2-dimensional SVM [15], which is summarized in Figure (II. 2).

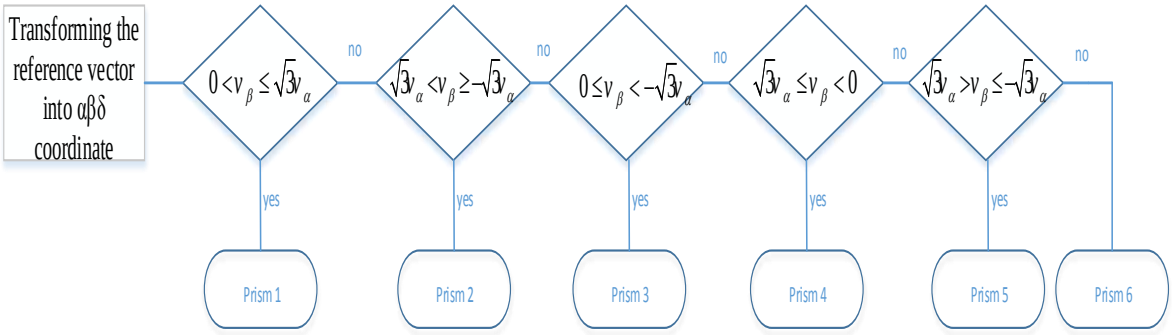


Figure (II. 2): Organogram of prism identification

Step 2: Tetrahedron identification

The next step is to determine the tetrahedron number according to the location of the reference voltage. As shown in Figure (II.3), each tetrahedron is limited from the top and the bottom by two planes.

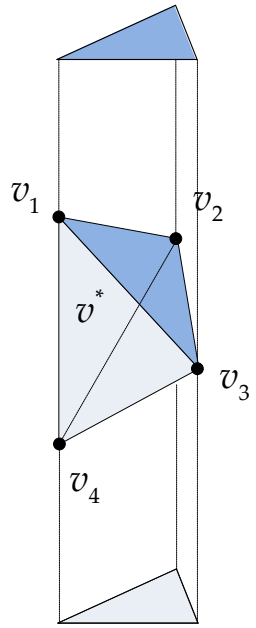


Figure (II.3): Example of a tetrahedron in a given prism

Each plane is created by three switching vectors. For example, the tetrahedron shown in Figure (II. 3), the top plane is formed by v_1, v_2 and v_3, and bottom plane is formed by v_2, v_3 and v_4. Equations of the top and bottom planes are written in the following form:

$$\begin{aligned} v_\gamma^* &= a_1 v_\alpha^* + b_1 v_\beta^* + c_1 \\ v_\gamma^* &= a_2 v_\alpha^* + b_2 v_\beta^* + c_2 \end{aligned} \tag{II.3}$$

Where: a_1, a_2, b_1, b_2, c_1, c_2 are constants, calculated by solving the equations (II.3) and (II.4):

$$\begin{bmatrix} v_{1\alpha} & v_{1\beta} & 1 \\ v_{2\alpha} & v_{2\beta} & 1 \\ v_{3\alpha} & v_{3\beta} & 1 \end{bmatrix} \begin{bmatrix} a_1 \\ b_1 \\ c_1 \end{bmatrix} = \begin{bmatrix} v_{1\gamma} \\ v_{2\gamma} \\ v_{3\gamma} \end{bmatrix} \tag{II.4}$$

$$\begin{bmatrix} v_{2\alpha} & v_{2\beta} & 1 \\ v_{3\alpha} & v_{3\beta} & 1 \\ v_{4\alpha} & v_{4\beta} & 1 \end{bmatrix} \begin{bmatrix} a_2 \\ b_2 \\ c_2 \end{bmatrix} = \begin{bmatrix} v_{2\gamma} \\ v_{3\gamma} \\ v_{4\gamma} \end{bmatrix} \quad \text{(II.5)}$$

Where: $v_{i\alpha}, v_{i\beta}$, and $v_{i\gamma}, i = 1,2,3 \text{ or } 4,$ are the components of the switching vector $v_{i\alpha}$ on $\alpha\beta$o plane.

The localization condition of this tetrahedron is given by:

$$\begin{aligned} v_\gamma^* &< a_1 v_\alpha^* + b_1 v_\beta^* + c_1 \\ v_\gamma^* &\geq a_2 v_\alpha^* + b_2 v_\beta^* + c_2 \end{aligned} \quad \text{(II.6)}$$

The localization condition of all tetrahedrons located in all prisms are summarized in table (A.4) of appendix.

II.2.2.2. Duration time calculation

In order to minimize the switching losses and to reduce the current ripple, switching vectors adjacent to the reference vector should be selected. At any sampling instant, the tip of the voltage vector lies in a tetrahedron formed by the four switching vectors. The on-duration time intervals of each vector are obtained in accordance to the average value principle, which is given by [16]:

$$\begin{aligned} v_1 t_1 + v_2 t_2 + v_3 t_3 + v_4 t_4 &= v^* T_s \\ t_1 + t_2 + t_2 + t_4 &= T_s \end{aligned} \quad \text{(II.7)}$$

Where T_s is the switching period, v_1, v_2, v_3 and v_4 are the four switching vectors adjacent to the reference voltage vector, and t_1, t_2, t_3 and t_4 are their on-duration time intervals respectively.

Expression (II.7) can by decomposed in the $\alpha\beta o$ coordinates system as follows:

$$\begin{bmatrix} v_{1\alpha} & v_{2\alpha} & v_{3\alpha} & v_{4\alpha} \\ v_{1\beta} & v_{2\beta} & v_{3\beta} & v_{4\beta} \\ v_{1o} & v_{2o} & v_{3o} & v_{4o} \\ 1 & 1 & 1 & 1 \end{bmatrix} \begin{bmatrix} t_1 \\ t_2 \\ t_3 \\ t_4 \end{bmatrix} = \begin{bmatrix} v_\alpha^* T_s \\ v_\beta^* T_s \\ v_o^* T_s \\ T_s \end{bmatrix} \tag{II.8}$$

The on duration time intervals are calculated by solving (II.23) for each tetrahedron:

$$\begin{bmatrix} t_1 \\ t_2 \\ t_3 \\ t_4 \end{bmatrix} = \begin{bmatrix} v_{1\alpha} & v_{2\alpha} & v_{3\alpha} & v_{4\alpha} \\ v_{1\beta} & v_{2\beta} & v_{3\beta} & v_{4\beta} \\ v_{1o} & v_{2o} & v_{3o} & v_{4o} \\ 1 & 1 & 1 & 1 \end{bmatrix}^{-1} \begin{bmatrix} v_\alpha^* T_s \\ v_\beta^* T_s \\ v_o^* T_s \\ T_s \end{bmatrix} \tag{II.23}$$

The table (II.1) summaries the on duration times and localization condition for the tetrahedrons located in prism1.

Table (II.1): On duration times and localization condition for all tetrahedron located in prism 1

Prism 1	*On duration time intervals*	*Condition of localisation*
Tetrahedron 1	$\begin{bmatrix} t_1 \\ t_2 \\ t_3 \end{bmatrix} = \begin{bmatrix} \frac{-\sqrt{6}}{3} & -\frac{\sqrt{2}}{2} & \frac{\sqrt{2}}{3} \\ 0 & \sqrt{2} & 0 \\ \frac{\sqrt{6}}{2} & -\frac{\sqrt{2}}{2} & 0 \end{bmatrix} \begin{bmatrix} v_\alpha^* T_s \\ v_\beta^* T_s \\ v_o^* T_s \end{bmatrix} \times \frac{1}{v_{dc}}$ $T_4 = T_s - T_1 - T_2 - T_3$	$v_\gamma \le -\sqrt{2} v_a + \sqrt{3} v_{dc}$ $v_\gamma > \frac{v_a}{\sqrt{2}} + \sqrt{\frac{3}{2}} v_\beta$
Tetrahedron 2	$\begin{bmatrix} t_1 \\ t_2 \\ t_3 \end{bmatrix} = \begin{bmatrix} -\frac{\sqrt{6}}{6} & \frac{\sqrt{2}}{2} & \frac{\sqrt{3}}{3} \\ \frac{\sqrt{6}}{2} & -\frac{\sqrt{2}}{2} & 0 \\ \frac{\sqrt{6}}{2} & \frac{\sqrt{2}}{2} & -\frac{\sqrt{3}}{3} \end{bmatrix} \begin{bmatrix} v_\alpha^* T_s \\ v_\beta^* T_s \\ v_o^* T_s \end{bmatrix} \times \frac{1}{v_{dc}}$ $T_4 = T_s - T_1 - T_2 - T_3$	$v_\gamma \le \frac{v_a}{\sqrt{2}} + \sqrt{\frac{3}{2}} v_\beta$ $v_\gamma > \frac{v_a}{\sqrt{2}} - \sqrt{\frac{3}{2}} v_\beta$
Tetrahedron 3	$\begin{bmatrix} t_1 \\ t_2 \\ t_3 \end{bmatrix} = \begin{bmatrix} -\frac{\sqrt{6}}{3} & 0 & \frac{\sqrt{3}}{3} \\ 0 & \sqrt{2} & 0 \\ \frac{\sqrt{6}}{6} & -\frac{\sqrt{2}}{2} & -\frac{\sqrt{3}}{3} \end{bmatrix} \begin{bmatrix} v_\alpha^* T_s \\ v_\beta^* T_s \\ v_o^* T_s \end{bmatrix} \times \frac{1}{v_{dc}}$ $T_4 = T_s - T_1 - T_2 - T_3$.	$v_\gamma \le \frac{v_a}{\sqrt{2}} - \sqrt{\frac{3}{2}} v_\beta$ $v_\gamma > -\sqrt{2} v_\alpha$
Tetrahedron 4	$\begin{bmatrix} t_1 \\ t_2 \\ t_3 \end{bmatrix} = \begin{bmatrix} 0 & \sqrt{2} & 0 \\ \frac{\sqrt{6}}{2} & -\frac{\sqrt{2}}{2} & 0 \\ -\frac{\sqrt{6}}{3} & 0 & -\frac{\sqrt{3}}{3} \end{bmatrix} \begin{bmatrix} v_\alpha^* T_s \\ v_\beta^* T_s \\ v_o^* T_s \end{bmatrix} \times \frac{1}{v_{dc}}$ $T_4 = T_s - T_1 - T_2 - T_3$	$v_\gamma \le -\sqrt{2} v_\alpha$ $v_\gamma \le \frac{v_a}{\sqrt{2}} + \sqrt{\frac{3}{2}} v_\beta - \sqrt{3} v_{dc}$

The duration times of the tetrahedrons located in all prisms are summarized in table (A.4) of appendix.

II.2.2.3. Pulses generation

By choosing the four adjacent switching vectors to create the reference voltage vector, it is possible to minimize the harmonic content of the switched waveforms. The main problem is how to put them in collation during switching period to minimize switching transitions and optimize the harmonic profile of the output voltage [17]. The adopted symmetrical switching sequence is widely used.

Figure (II.4) shows the pulses generation of four tetrahedrons located in the prism 1

The switching period is divided into ten segments to split the applying time of each switching vector evenly.

The modulation period always starts by applying the zero switching vector (0000), the next applied switching vector is selected so that only one switch state is changed at a time, after the first, second and the third active switching vectors are applied, the other zero switching vector (1111) is followed. After these steps, the sequence is repeated in a reverse order.

The Table (II.2) presents the order of the switching vectors in which they should be applied to minimize the state changes during a modulation period.

Table (II.2): Order of the switching vectors for four-leg inverter

		Switching vectors									
Sector 1	***TeT 1***	0000	1000	1100	1110	1111	1111	1110	1100	1000	0000
	TeT 2	0000	1000	1100	1101	1111	1111	1101	1100	1000	0000
	TeT 3	0000	1000	1001	1101	1111	1111	1101	1001	1000	0000
	TeT 4	0000	0001	1001	1101	1111	1111	1101	1001	0001	0000
Sector 2	***TeT 1***	0000	0100	1100	1110	1111	1111	1110	1100	0100	0000
	TeT 2	0000	0100	1100	1101	1111	1111	1101	1100	0100	0000
	TeT 3	0000	0100	1101	1101	1111	1111	1101	0101	0100	0000
	TeT 4	0000	0001	0101	1101	1111	1111	1101	0101	0001	0000
Sector 3	***TeT 1***	0000	0100	0110	1110	1111	1111	1110	0110	0100	0000
	TeT 2	0000	0100	0110	0101	1111	1111	0101	0110	0100	0000
	TeT 3	0000	0111	0110	0101	1111	1111	0101	0110	0111	0000
	TeT 4	0000	0001	0101	0111	1111	1111	0111	0101	0001	0000
Sector 4	***TeT 1***	0000	0010	0110	1110	1111	1111	1110	0110	0010	0000
	TeT 2	0000	0010	0110	0111	1111	1111	0111	0110	0010	0000
	TeT 3	0000	0010	0011	0111	1111	1111	0111	0011	0010	0000
	TeT 4	0000	0001	0011	0111	1111	1111	0111	0011	0001	0000
Sector 5	***TeT 1***	0000	0010	1010	1110	1111	1111	1110	1010	1110	0000
	TeT 2	0000	0010	1010	1011	1111	1111	1011	1010	0010	0000
	TeT 3	0000	0010	0010	1011	1111	1111	1011	0010	0010	0000
	TeT 4	0000	0001	0011	1011	1111	1111	1011	0011	0001	0000
Sector 6	***TeT 1***	0000	1000	1010	1110	1111	1111	1110	1010	1000	0000
	TeT 2	0000	1000	1010	1011	1111	1111	1011	1010	1000	0000
	TeT 3	0000	1000	1001	1011	1111	1111	1011	1001	1000	0000
	TeT 4	0000	0001	1001	1011	1111	1111	1011	1001	0001	0000
		Switching period T_s									

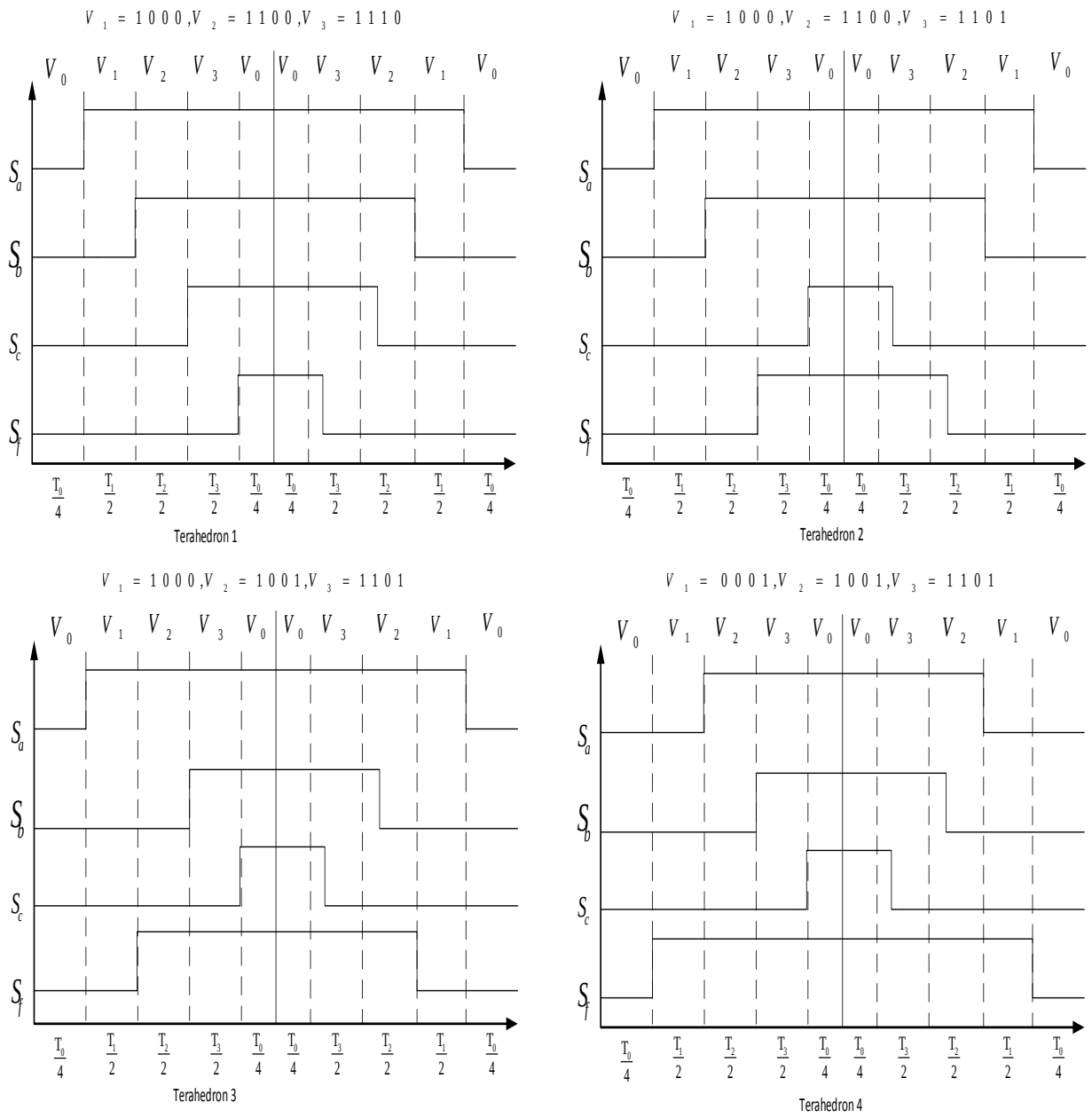


Figure (II.4): Symmetrical pulses of the tetrahedrons of the first prism

Finely, the implementation procedure of the 3DSVM algorithm is summarized in figure (II.5).

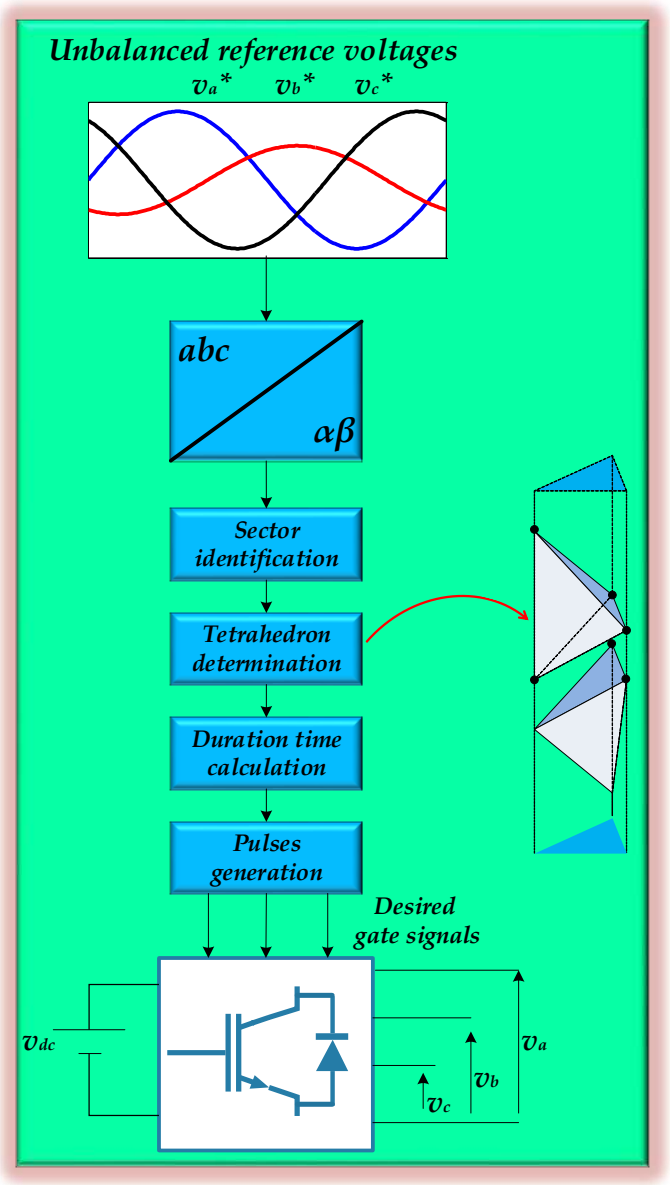


Figure (II.5): Three-dimensional space vector modulation algorithm

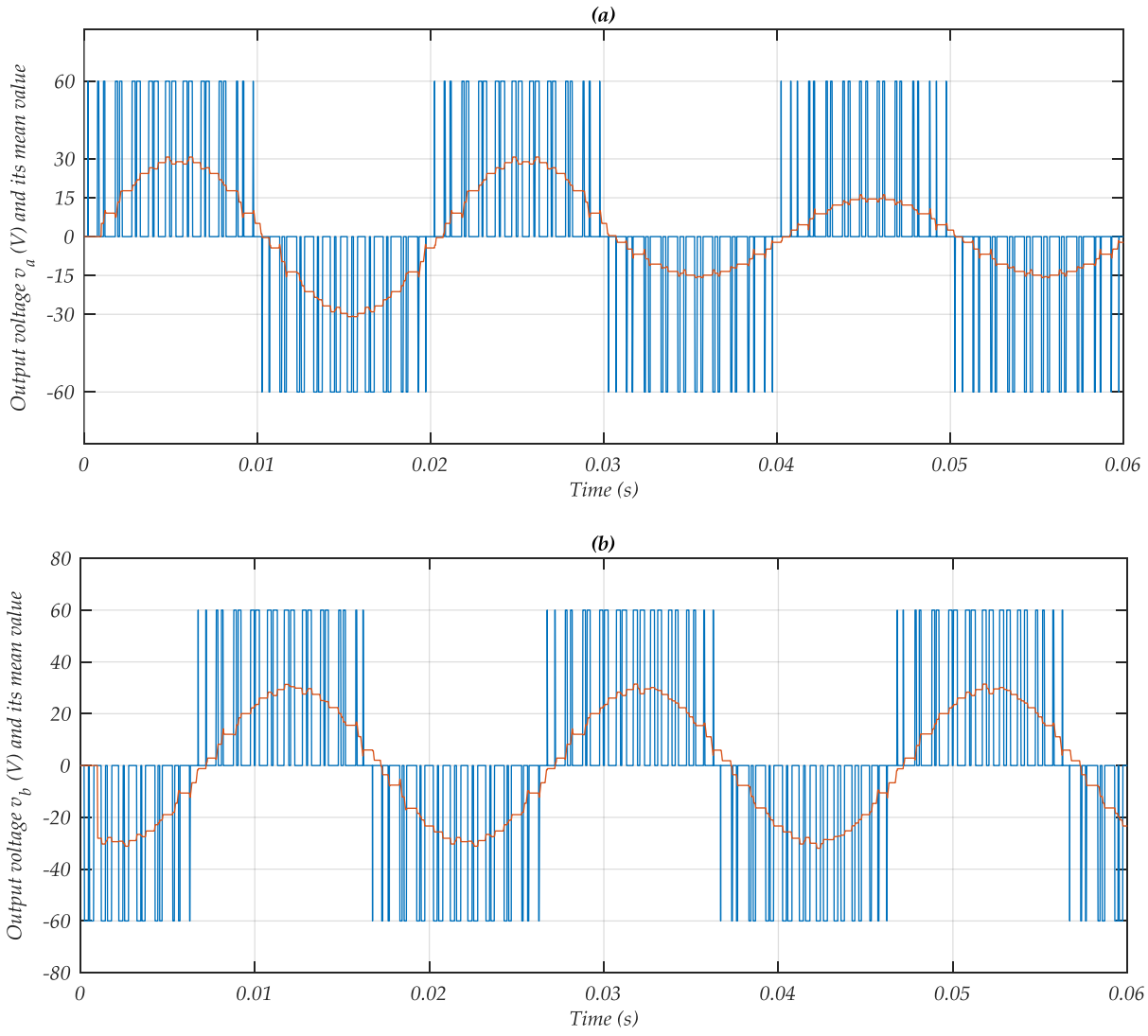
II.3. Simulation results

The inverter's load is an inductive load (R=500Ω, L=0.4H), and the input DC voltage of the inverter is set to v_{dc} = 60 V.

After 0.03 s, the amplitude of the reference voltage of phase (a) is reduced to 50% in order to induce an unbalanced reference voltage.

Figures (II.6), (II.7) and (II.8) show the waveforms of the output voltages and currents of the four-leg inverter operated at the switching frequencies 1, 2 and 5 kHz respectively. These results are consistent with the analytical waveforms and demonstrate feasibility and efficiency of the 3DSVM for four-leg inverter under balanced and unbalanced reference voltages conditions. It can be observed also that the quality of the voltage and current waveforms are improved when the switching frequency is increased.

The frequency spectrum of load of the a-phase are presented in Figure (II.9). One notices well that the THD decreases remarkably with increase of the switching frequency.



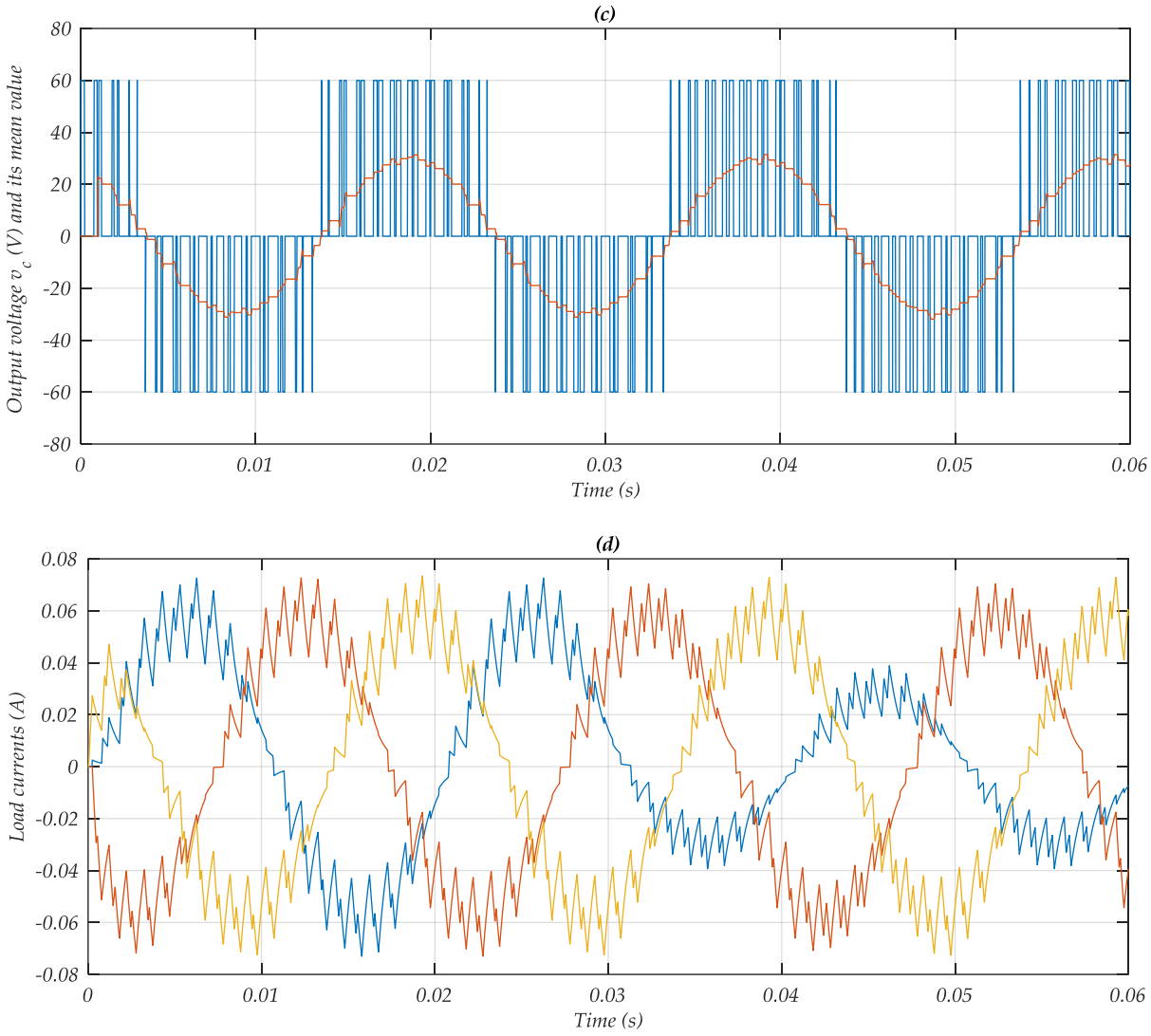
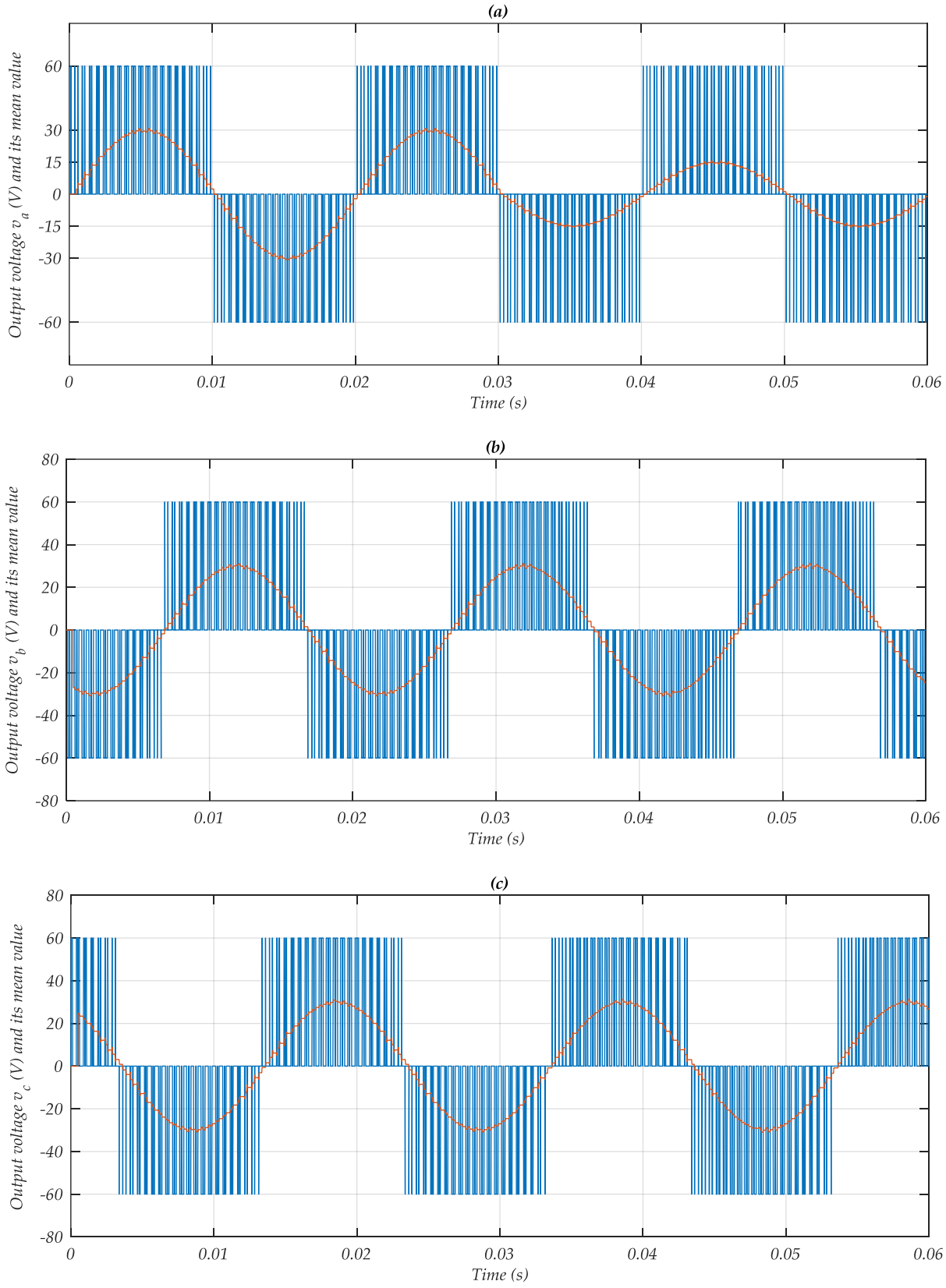


Figure (II.6): Output voltages and currents waveforms of a two-level four-leg inverter with switching frequency 1 kHz


(a)
Output voltage v_a (V) and its mean value
60
30
15
0
-15
-30
-60
0
0.01
0.02
0.03
0.04
0.05
0.06
Time (s)
(b)
Output voltage v_b (V) and its mean value
80
60
40
20
0
-20
-40
-60
-80
0
0.01
0.02
0.03
0.04
0.05
0.06
Time (s)
(c)
Output voltage v_c (V) and its mean value
80
60
40
20
0
-20
-40
-60
-80
0
0.01
0.02
0.03
0.04
0.05
0.06
Time (s)

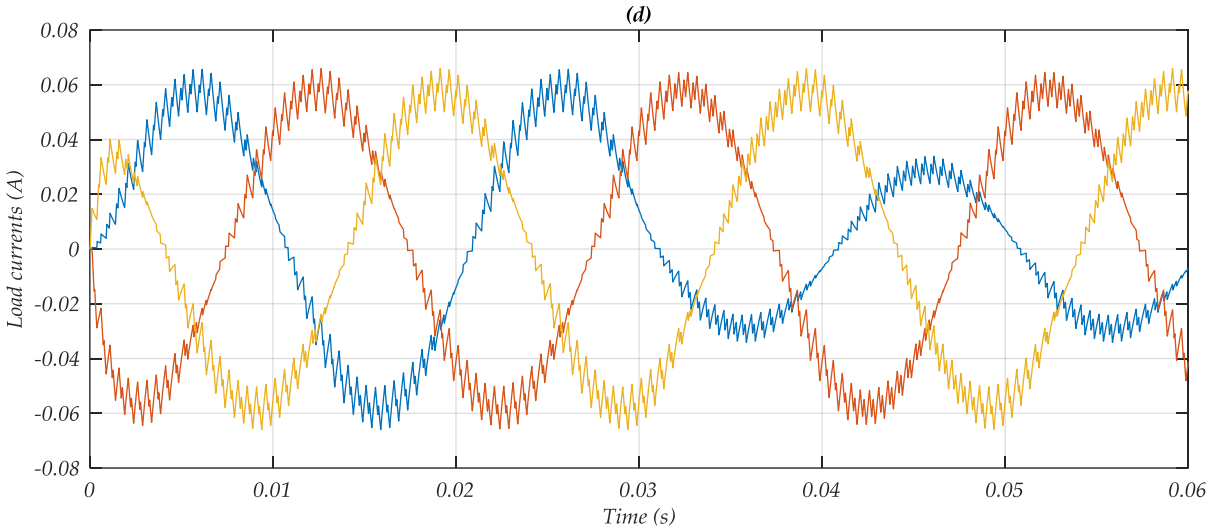
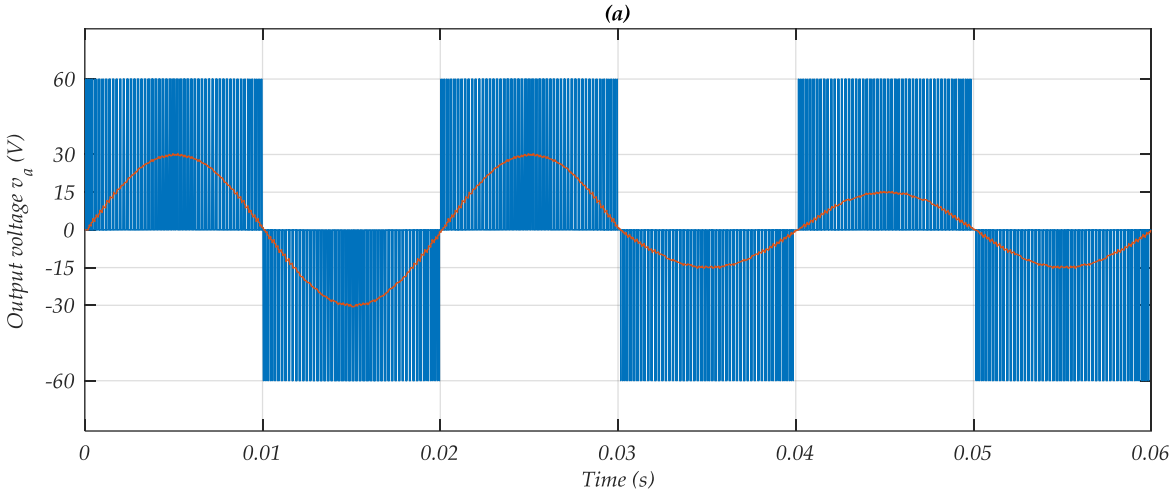


Figure (II.7): Output voltages and currents waveforms of a two-level four-leg inverter with switching frequency 2 kHz



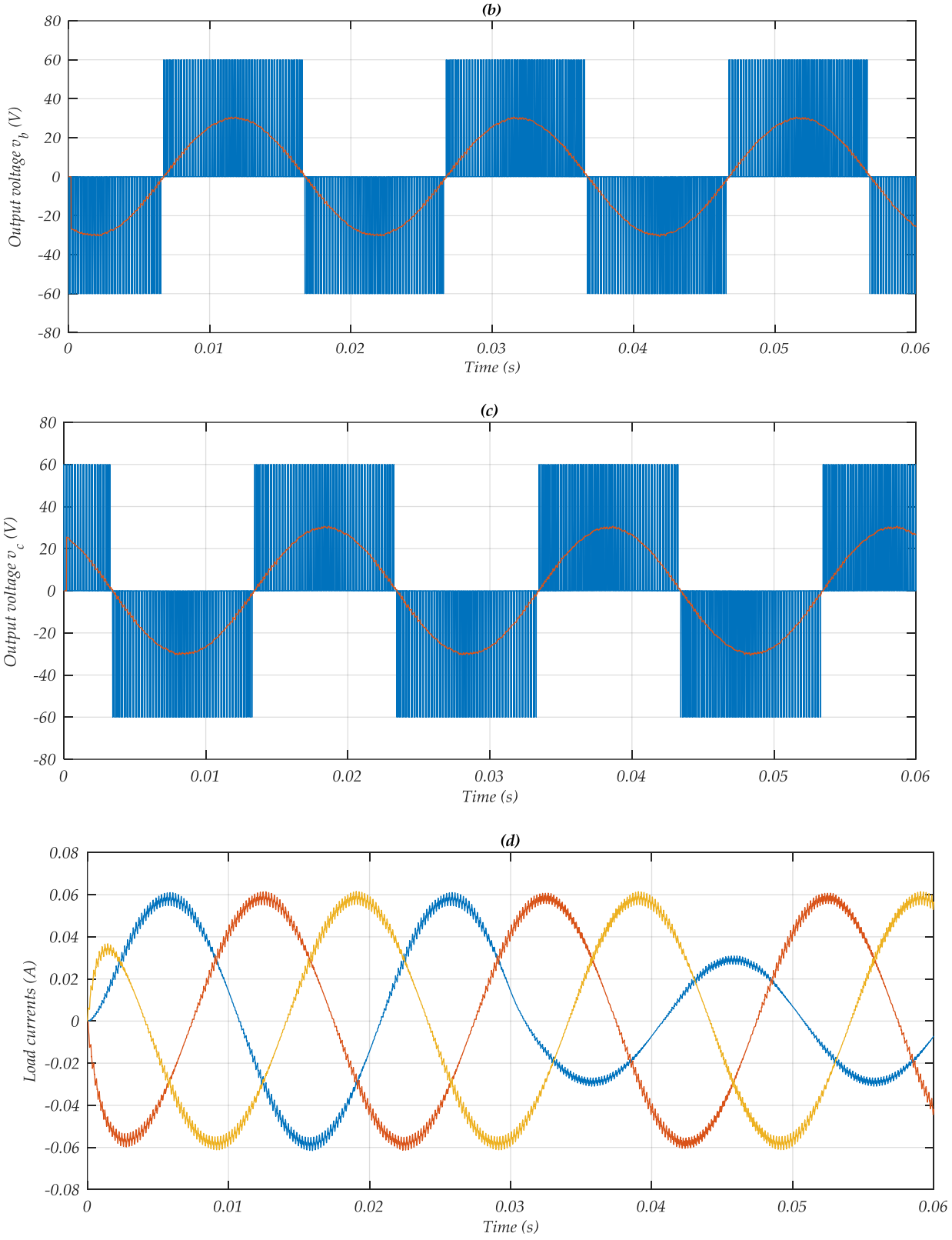


Figure (II.8): Output voltages and currents waveforms of a two-level four-leg inverter with switching frequency 5 kHz

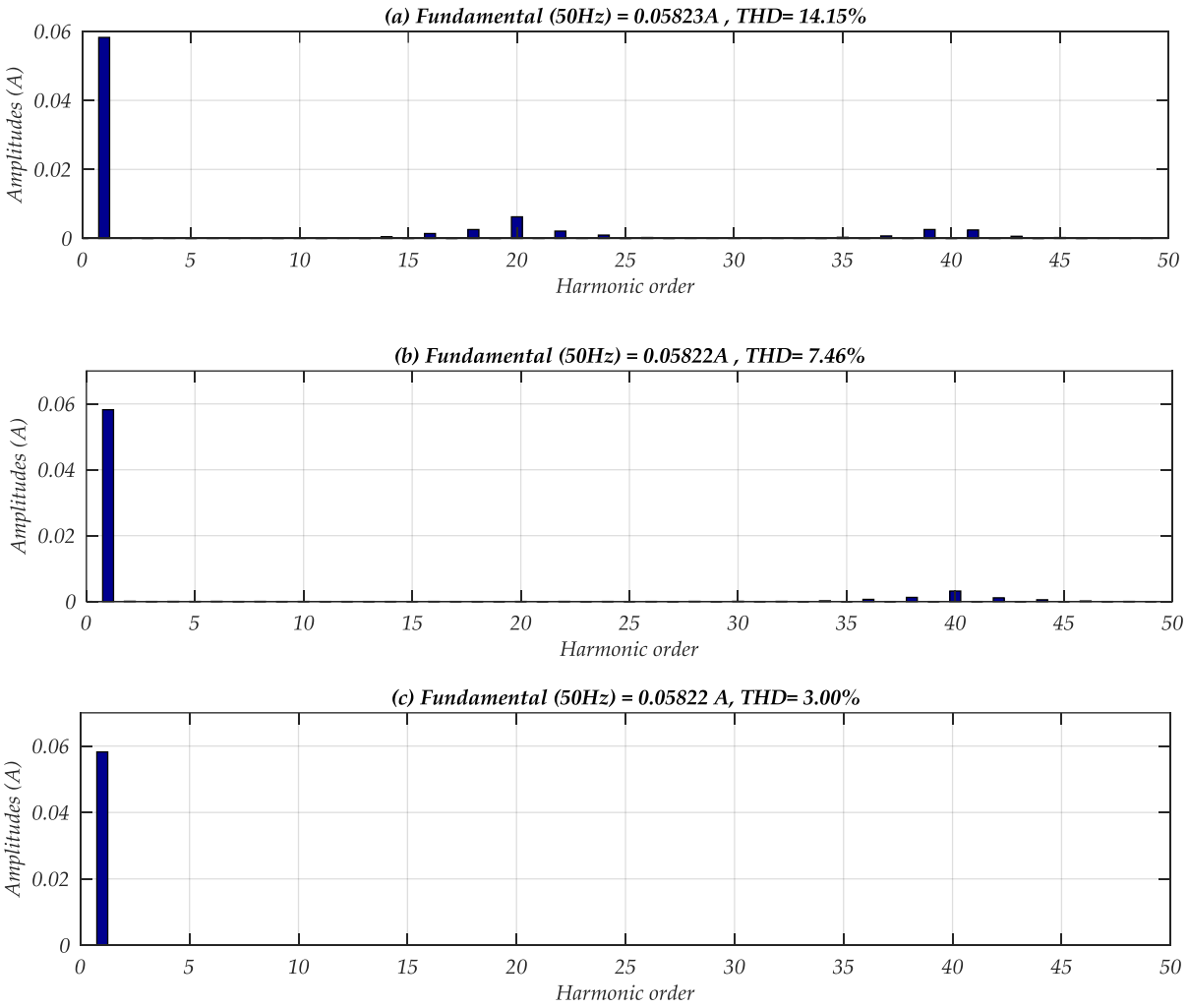


Figure (II.9): Frequency spectrum of the load current, (a): With switching frequency 1 kHz, (b): With switching frequency 2 kHz, (c): With switching frequency 5 kHz

II.4. Conclusion:

In this chapter, the three-dimensional space vector modulation for four-leg inverter is presented. A comprehensive procedure for 3D SVM is performed in detail, which includes identification of the reference voltage vector location in the 3-D space, computing the switching vector duration times, and gate drive signal derivation. The simulation results demonstrate that the 3DSVM is very suitable for control of four-leg voltage source inverters under balanced and unbalanced reference voltages conditions.

The next chapter will be reserved to the implementation of the 3DSVM for four-leg inverter using FPGA technology.

Chapter III:

FPGA-Based control of three-phase four-leg inverter

III.1. Introduction

The increasing progress in power converters in power electronics applications require capable digital processors. In order to satisfy most of these requirements, recent research studies proved that the field programmable gate arrays (FPGA) are an appropriate alternative over digital signal processors (DSP) and micro controllers [17].

Alternatively, the advanced FPGA may provide multiple PWM gate signals according to the system requirements. Moreover, the DSP/microcontroller runs a sequential program in its microprocessor and FPGA runs all the operations in parallel with the clock pulse. Thus, the FPGA may update all gate pulses of the switching controller simultaneously. The ability of parallel operation makes the processing time independent of the number

of converter levels. Therefore, the FPGA-based switching control technology could be the first choice for power electronics converters [18].

III.2. FPGA generic architecture description

FPGAs belong to the wide family of programmable logic components. An FPGA is defined as a matrix of configurable logic blocks (CLBs) (combinatorial and/or sequential), linked to each other by an interconnection network which is entirely reprogrammable. The memory cells control the logic blocks as well as the connections so that the component can fulfill the required application specifications [19].

Several configurable technologies exist. Among them, only those that are reprogrammable (Flash, EPROM, SRAM) are of interest since they allow the same flexibility as that of a microprocessor. The generic architecture of an SRAM-based FPGA is presented in Figure (III.1). The most recent FPGAs are produced using a 65-nm copper process [19]. Their density can reach more than 10 million equivalent gates per chip with clock system frequencies of more than 500 MHz However, it is important to note that this kind of information is only accurate for a short while as technology continues to move forward. The two main FPGA manufacturers are Altera and Xilinx[20],[21].

The FPGA generic architecture is composed of a matrix of CLBs, where the number of rows and columns is now reaching, for the largest devices, 192 × 116. A ring of configurable input/output blocks (IOBs), whose number can reach 1000 user IOBs, borders this matrix core. Finally, all these resources communicate among themselves through a programmable interconnection network. It consists of the following fundamental programmable functional elements [22].

1) ***Configurable Logic Blocks (CLBs):*** Their structures include two, four, or more logic cells, also called logic elements. The structure of a logic cell, which can be

considered as the basic grain of the FPGA, is presented in figure (III. 2). It consists of a four-bit lookup table (LUT), which can be configured either as a (16 × 1) ROM, RAM, or a combinatorial function. A carry look-ahead data path is also included in order to build efficient arithmetic operators. Finally, a D-type flip-flop, with all its control inputs (synchronous or asynchronous set/reset, enable), allows registering the output of the logic cell. Such architecture corresponds to a microstate machine, since the registered output can be configured as an input of the same logic cell [19].

2) ***Input/output Blocks (IOBs):*** control the flow of data between the I/O pins and the internal logic of the device. IOBs support bidirectional data flow plus 3-state operation. They support a variety of signal standards including several high performance differential standards and Double Data Rate (DDR) registers. Block RAM provides data storage in the form of 18-Kb dual-port blocks [19].
3) ***Digital Clock Manager (DCM):*** Blocks provide self-calibrating, fully digital solutions for distributing, delaying, multiplying, dividing and phase shifting clock signals [20].
4) ***A Rich Routing network:*** that interconnects all five functional elements, transmitting signals among them. Each functional element has an associated witch matrix that permits multiple connections to the routing [20].

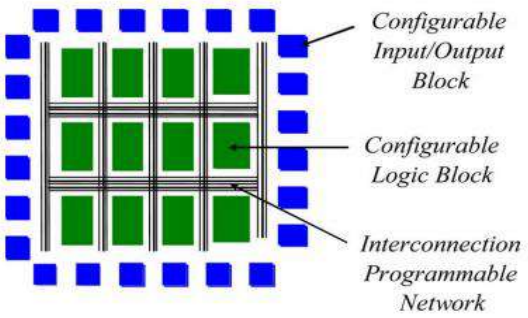


Figure (III.1): Generic architecture of an FPGA

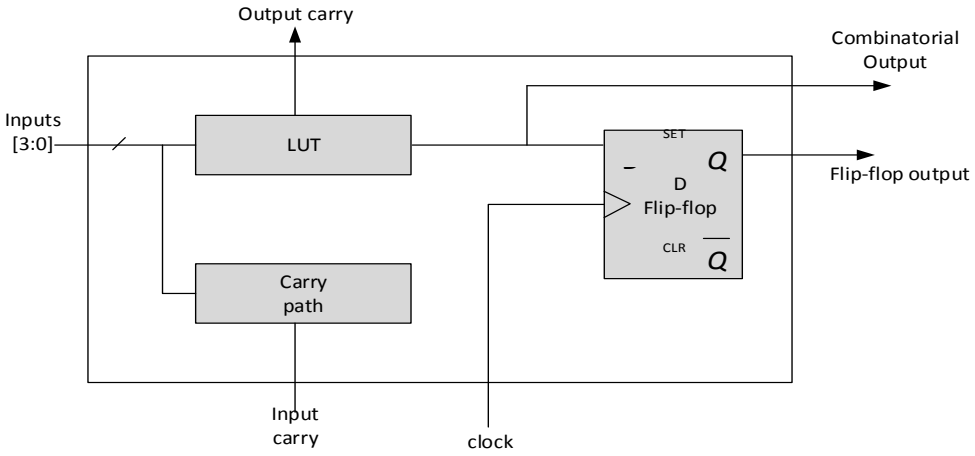


Figure (III.2): Logic cell structure

III.2.1. FPGA design flows

The designer facing a design problem must go through a series of steps between initial ideas and final hardware. This series of steps is commonly referred to as the "design flow" (see Figure (III.3). First, after all the requirements have been spelled out, a proper digital design phase must be carried out. It should be stressed that the tools supplied by the different FPGA vendors to target their chips do not help the designer in this phase. They only enter the scene once the designer is ready to translate a given design into working hardware [23].

The most common flow nowadays used in the design of FPGAs involves the following subsequent phases [23]:

1- ***Design entry:*** There are different techniques for design entry, schematic based, Hardware Description Language and combination of both etc. Selection of a method depends on the design and designer. If the designer wants to deal more with Hardware, then Schematic entry is the better choice. When the design is complex or the designer thinks the design in an algorithmic way then HDL is the better choice.

2- ***Synthesis***: The process, which translates VHDL or Verilog code into a device netlist format i.e. a complete circuit with logical elements (gates, flip-flops, etc…) for the design. If the design contains more than one sub designs, ex. to implement a processor, we need a CPU as one design element and RAM as another and so on, and then the synthesis process generates netlist for each design element. Synthesis process will check code syntax and analyze the hierarchy of the design which ensures that the design is optimized for the design architecture, the designer has selected. The resulting netlist(s) is saved to an NGC (Negative Generic Circuit) file (for Xilinx® Synthesis Technology (XST)) [23].

3- ***Implementation***: This process consists a sequence of three steps: Translate Map, Place and Route.

Translate process combines all the input netlists and constraints to a logic design file. This information is saved as a NGD (Negative Generic Database) file. This can be done using NGD Build program. Here, defining constraints is nothing but, assigning the ports in the design to the physical elements (ex. pins, switches, buttons etc.) of the targeted device and specifying time requirements of the design. This information is stored in a file named UCF (User Constraints File) [19].

Map process divides the whole circuit with logical elements into sub blocks such that they can be fit into the FPGA logic blocks. That means map process fits the logic defined by the NGD file into the targeted FPGA elements (Combinational Logic Blocks (CLB), Input Output Blocks (IOB)) and generates an NCD (Native Circuit Description) file, which physically represents the design mapped to the components of FPGA [23].

The place and route process places the sub blocks from the map process into logic blocks according to the constraints and connects the logic blocks. If a sub block is placed in a logic block, which is very near to IO pin, then it may save the time but it may effect some other constraint. Therefore, tradeoff between all the constraints is taken account by the place and route process [23].

4- ***Device Programming:*** Now the design must be loaded on the FPGA. But the design must be converted to a format so that the FPGA can accept it. BITGEN program deals with the conversion. The routed NCD file is then given to the BITGEN program to generate a bit stream (a .BIT file) which can be used to configure the target FPGA device. This can be done using a cable. Selection of cable depends on the design [23].

5- ***Design Verification:*** Verification can be done at different stages of the process steps.

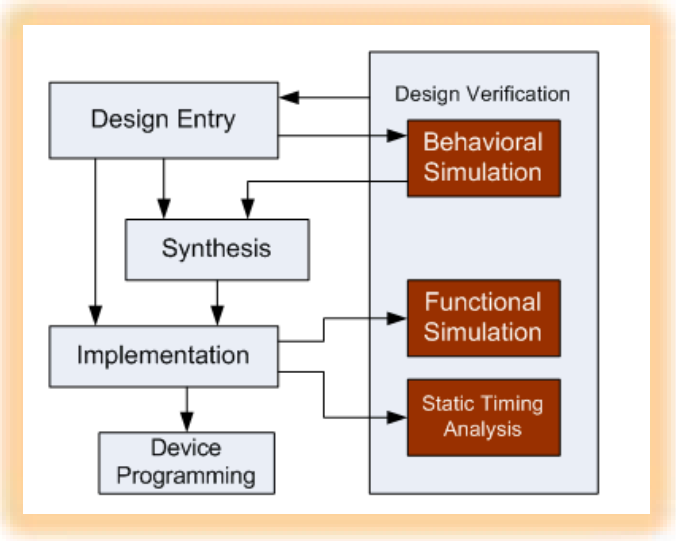


Figure (III. 3): Xilinx FPGA design flow

III.3. Implementation of 3DSVM based on FPGA for four-leg inverter

In present work, the Xilinx ZedBoard Zynq-7000 development board is used to implement 3DSVM for four-leg inverter [24] The VHDL-code-based behavioral models of different 3DSVM blocks are designed and synthesized using the Project Navigator tool of the Xilinx ISE Design Suite 14.7 software. Figure (III. 4) shows the RTL schematic of 3DSVM algorithm, as we can see, there are four inputs:

- ***Clock (clk)*:** is the clock source of the FPGA board (100 MHz);
- ***Reset:*** to reset all outputs to zero when its value is '1'.
- ***Select of switching frequency (Choice):*** to change the switching frequency directly from the switches of the FPGA board.
- ***Balanced/Unbalanced voltages Mode*:** to make the generated voltages balanced or unbalanced directly from the switches of the FPGA board.

The outputs are eight gate pulses for three-phase four-leg inverter.

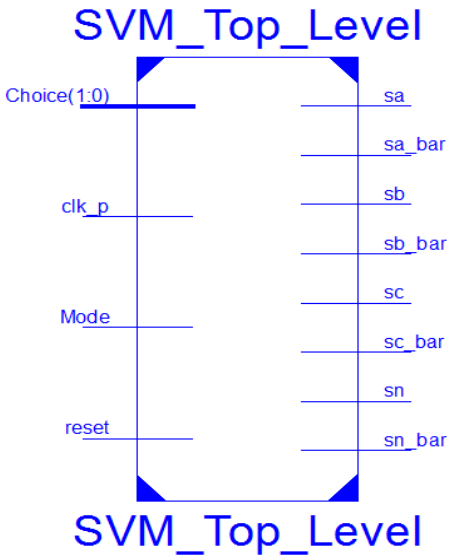


Figure (III. 4): RTL schematic of 3DSVM

As shown in figure (III. 5), the RTL schematic of figure (III. 4) is divided into the following blocks:

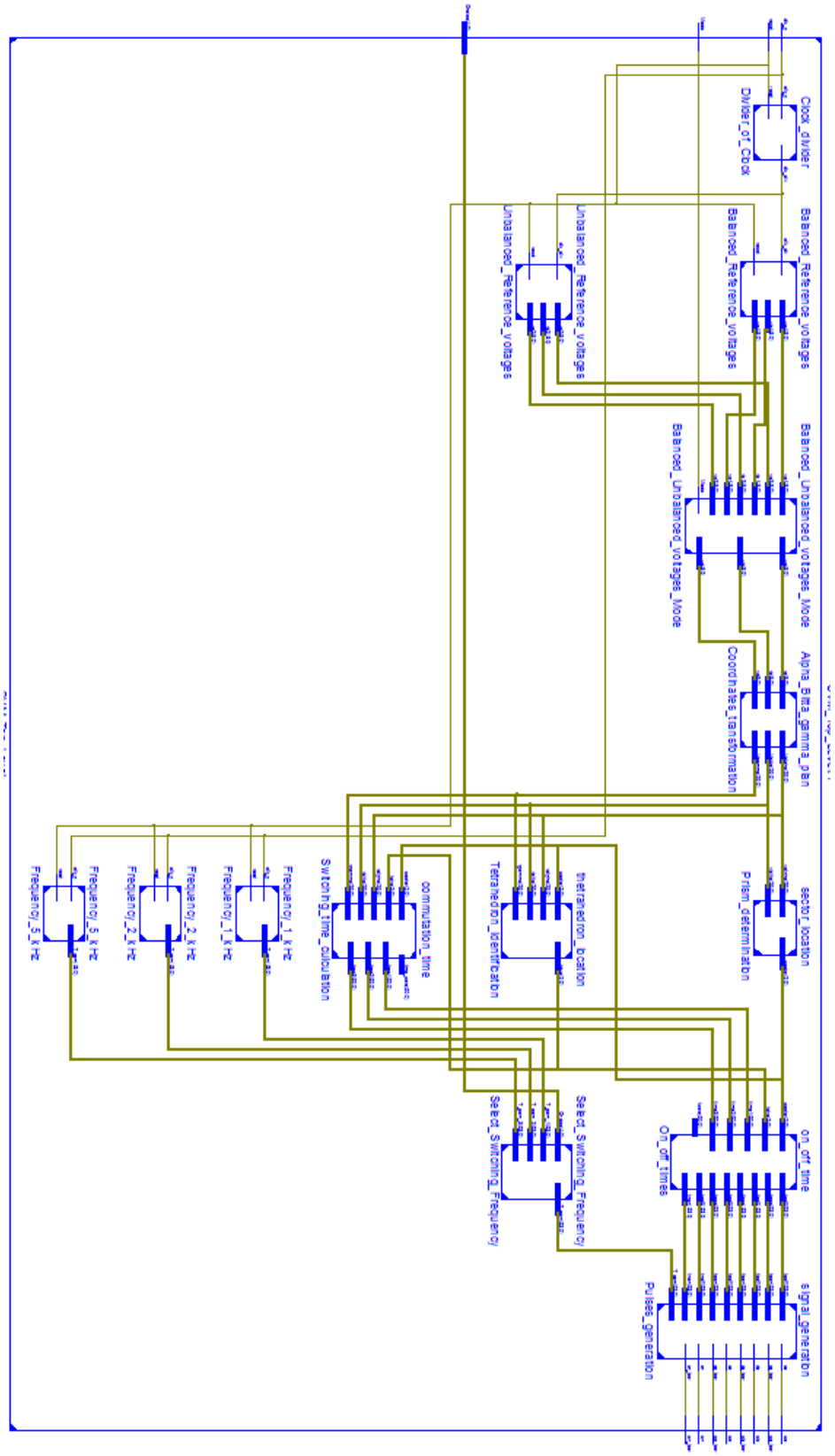


Figure (III. 5): RTL schematic inside of 3DSVM

1) ***Clock divider:*** Clock Divider is also known as frequency divider, which divides the input clock frequency and produce output clock. In our case, the input clock of the FPGA is 100MHz, which is divided to generate 50 Hz of the reference voltages at the next block.
2) ***Reference voltages generation*:** The three-phase reference voltages are programmed in this block. The reference voltages are generated by taking 600 samples within a period listed in table (array). At each rising edge of the clock, the output voltages take their sample values using the index (i) that varies from 0 to 599.
3) ***Coordinates transformation*:** the generated three-phase reference voltages are used in this block as inputs and their outputs are the reference voltages in $\alpha\beta\gamma$ coordinates $v_\alpha^* \quad v_\beta^* \quad v_\gamma^*$.
4) ***Prism determination*:** This block uses $v_\alpha^* \quad v_\beta^* \quad v_\gamma^*$ as inputs and determines the prism number of where the reference vector is located.
5) ***Tetrahedron identification***: Once the prism number is known, the number of tetrahedron should be identified. This block implements the comparison process described in chapter II (table (II. 1)) and uses both of reference voltages in $\alpha\beta\gamma$ coordinates and the prism number to obtain the tetrahedron number.
6) ***Switching time calculation*:** This block calculates the duration times of the adjacent switching vectors of a given tetrahedron and provides at its outputs the signals t_1, t_2, t_3 and t_4.
7) ***On-off time's intervals***: In order to generate gate pulse, the on time and off time should be calculated in each tetrahedron. This block uses the number of prism and tetrahedron that contain the reference voltage vector and the calculated switching times as inputs in order to deliver on and off times required to generate the pulses.

8) ***Pulses generation*:** This block creates the gate pulses of each switch of the four-leg inverter, which takes into account the dead times between the switches of same leg (Dead time = 4µs).
9) ***Select of switching frequency***: This block offer the possibility of change the switching frequency according to its input (choice). When the choice = "00", the switching frequency is 1 kHz, when "01" the switching frequency is 2kHz, for the remaining combinations of the choice, the switching frequency is 5kHz.

III.4. Experimental hardware setup of four-leg inverter based 3DSVM control

Figure (III. 6) shows the complete experimental hardware setup of four-leg inverter, which is divided in tow main part, control and power parts.

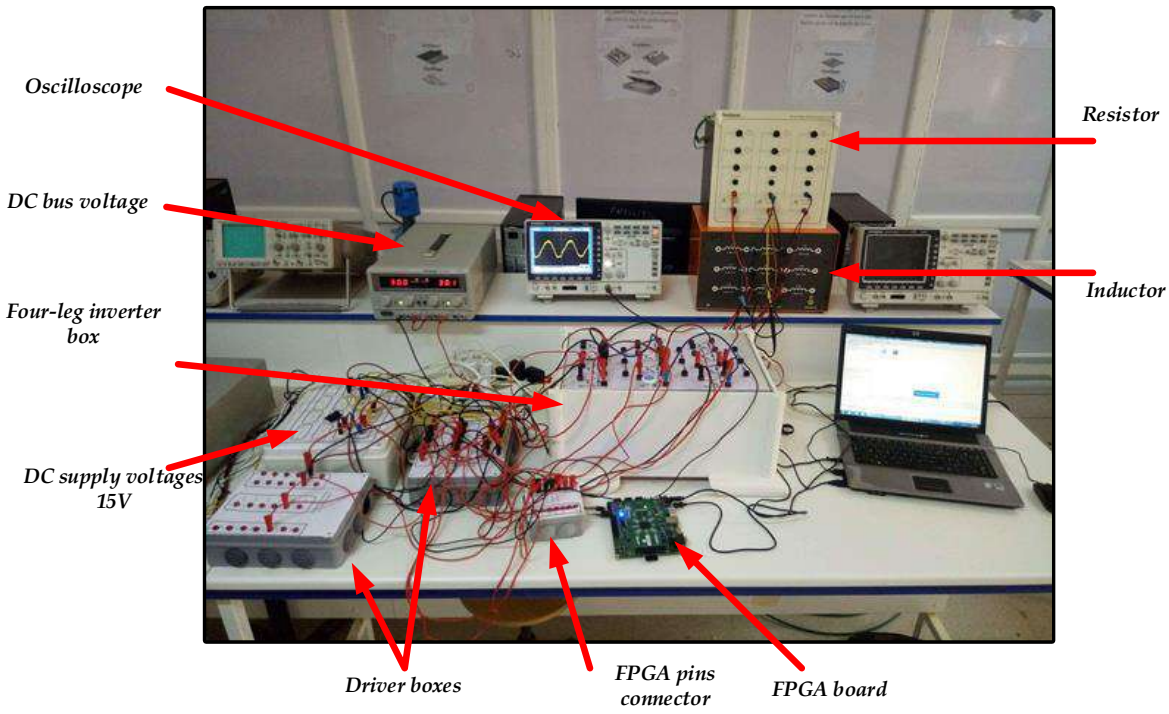


Figure (III. 6): Photograph of the complete experimental hardware setup of four-leg inverter based 3DSVM control

III.4.1. Power part

The used power components are described as follow:

***Three-phase four-leg inverter box*:** Figure (III. 7) shows the power circuit (inside and outside) of three-phase four-leg inverter, which composed of eight Insulated Gate Bipolar Transistor (8 IGBTs) IRGPS40B120U fabricated by International Rectifier [25].

1- ***Three-phase inductive load***: R = 500 Ω and L = 0.4 H (see figure (III. 6)).

2- ***DC power supply 60 V***: is used to feed the four-lrg inverter (see figure (III. 6)).

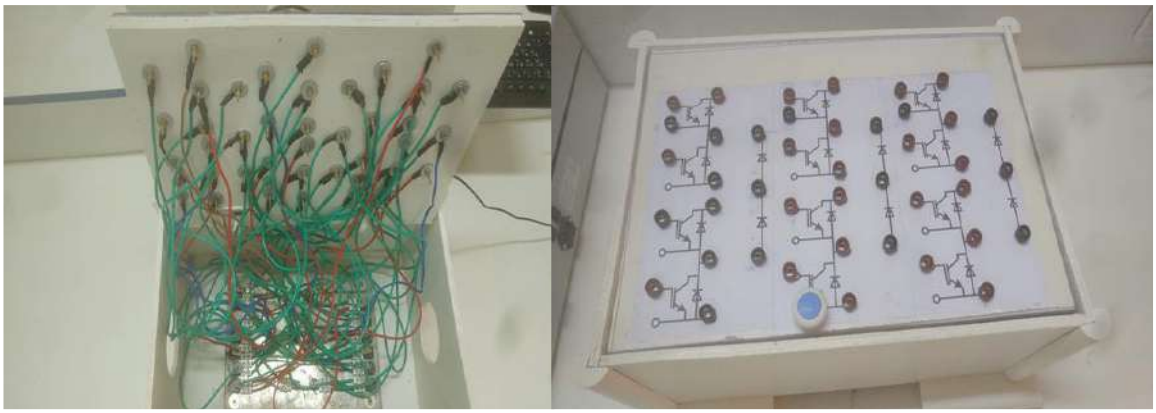


Figure (III. 7): Power circuit of three-phase four-leg inverter

III.4.2. Control part

1- ***Driver boxes:*** the pluses train generated form FPGA is only 3.3V, which is not enough to drive the IGBTs that need 15V. The HCPL-3120 driver [26] s used to amplify the signals generated from the FPGA and isolate this latter from the power circuit (see figure (III. 8)).

Figure (III. 9) shows schematic diagram of one driver for one IGBT, which contains the following components:

- HCPL-3120 Drivers;
- Two capacitors C_1 and C_2 of 1mF/63 V and 100 nF/35 V respectively;
- Voltage regulator L7815;
- Two resistances R_1 and R_2 of 300 Ω and 10 Ω.
- DC voltage of 5V.

Figure (III. 10) presents the photograph of six drivers placed in one box from outside and inside.

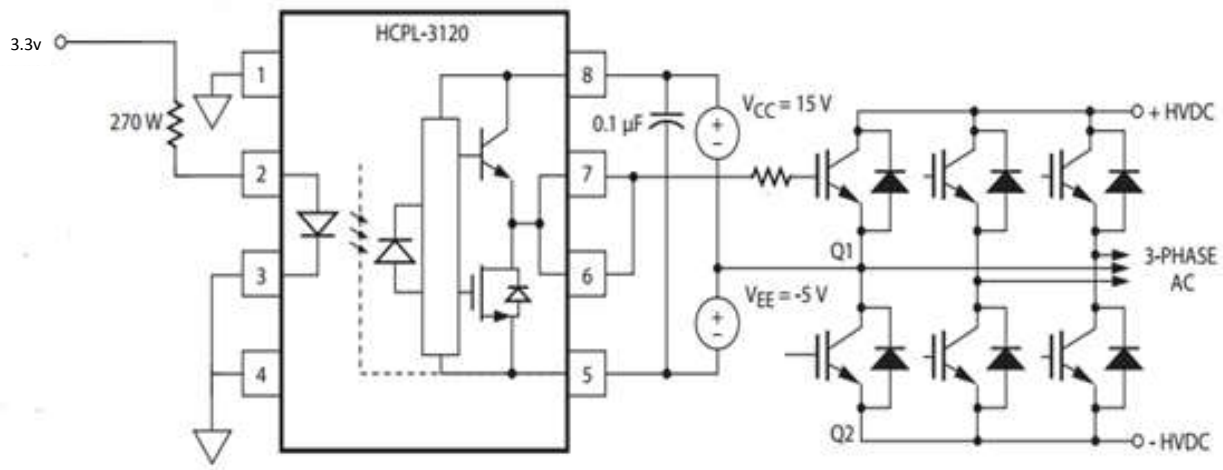


Figure (III. 8): HCPL-3120 Typical Application Circuit with Negative IGBT Gate Driv

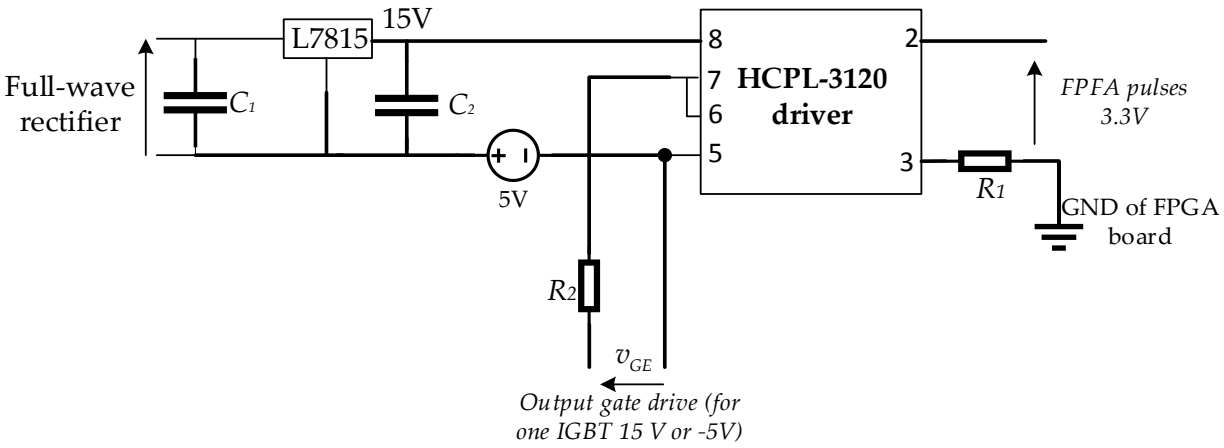


Figure (III. 9): Schematic circuit of one driver for one IGBT

(a) (b)

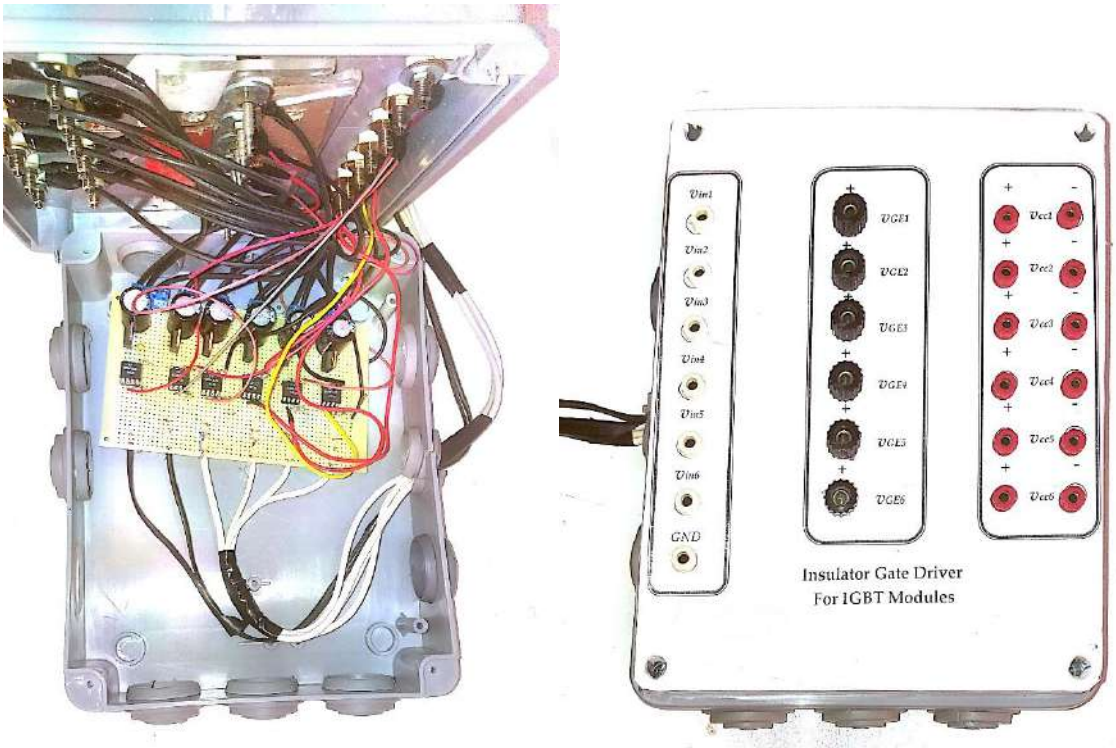


Figure (III. 10): Insulator Gate Driver box for six IGBTs Modules

(a): From outside, (b): from inside

2- ***DC Power supply 15V***: in order to supply the driver boxes, a conversion AC to DC is performed in this box (see figure (III. 11)). The components used in this box are:

- Eight transformers 220/12 V to reduce the AC voltage from 220V to 12V;
- Eight H-Bridge rectifiers KBPC3510 [27] o convert the AC voltage to DC voltage.

(a) (b)

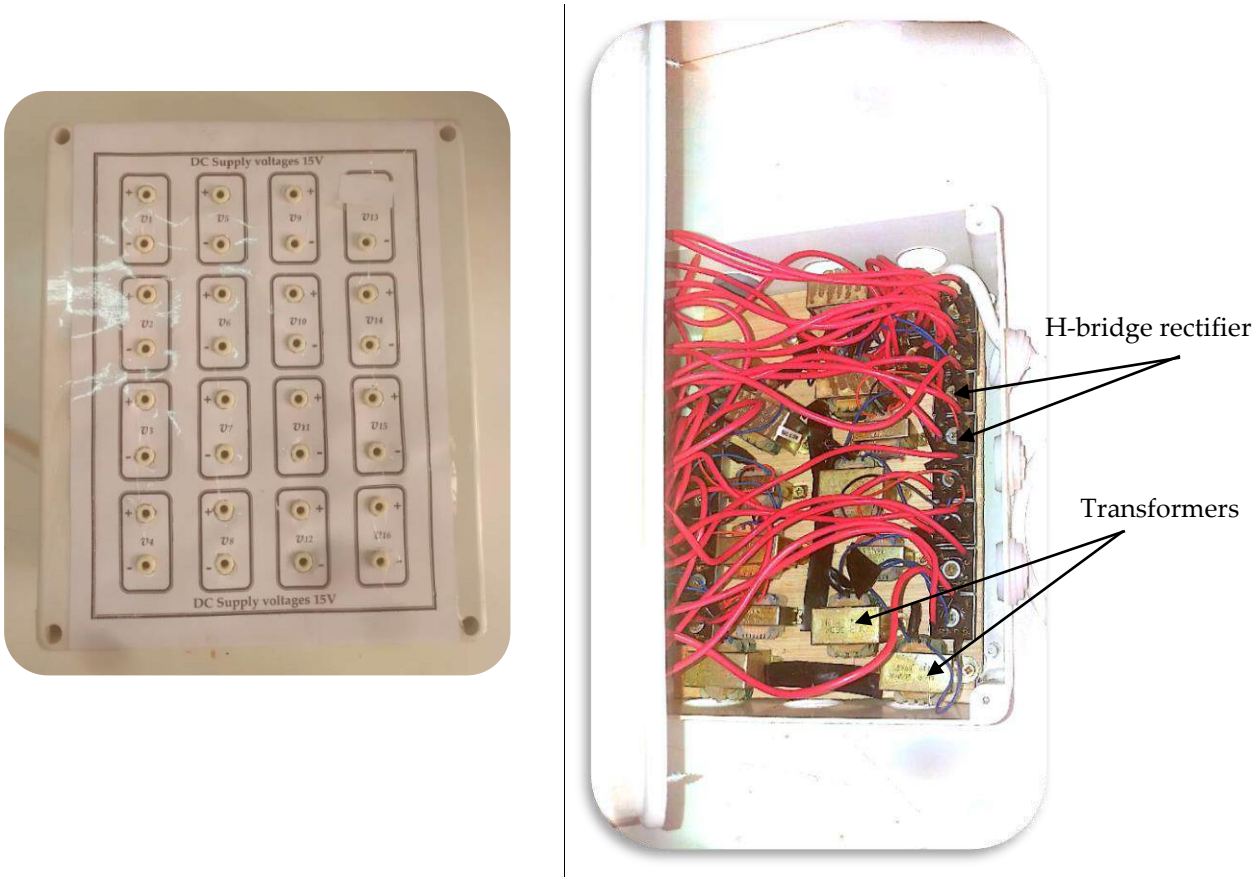


Figure (III. 11): The box of DC Supply voltages 15 V (a) from outside (b) from inside.

III.5. Experimental results and discussion

To verify the effectiveness of the 3DSVM, the three-phase four-leg inverter is operated under balanced and unbalanced reference voltages with different switching frequency. Figure (III. 12) illustrates the output gate pulse from FPGA and its corresponding of driver circuit under switching frequency of 5 kHz. As we can see, the delay between them is almost zero.

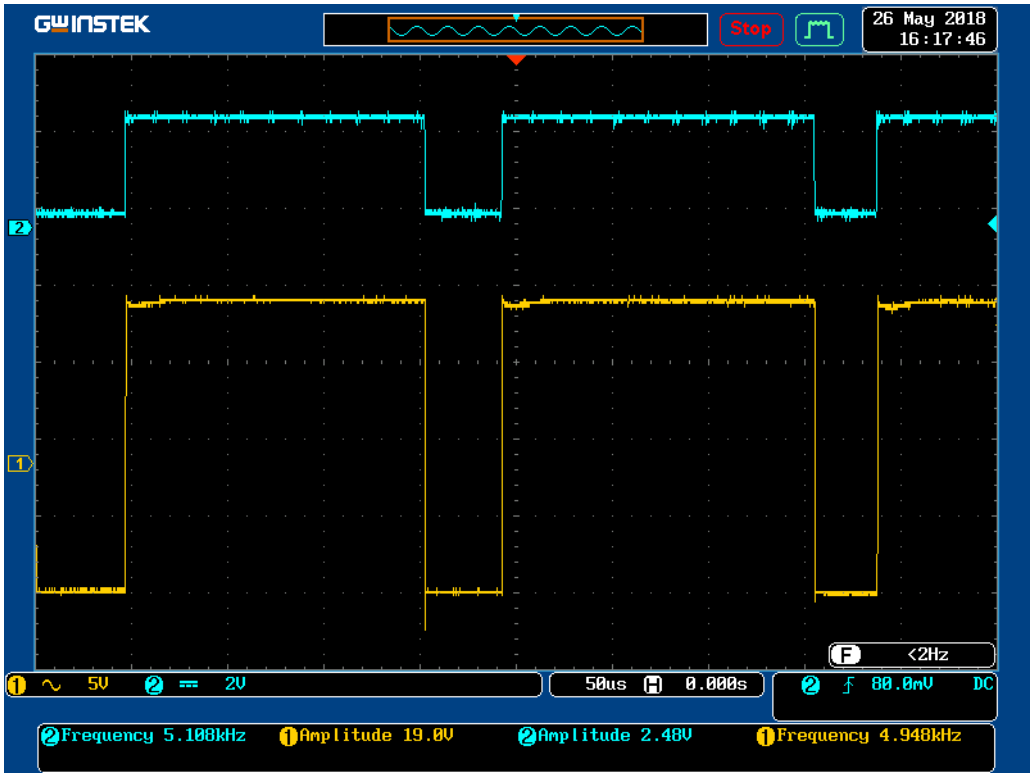


Figure (III. 12): Measured gate pulse from FPGA and driver circuit

The gate pulses of the upper and lower switches of one leg are shown in figure (III. 13). It can be seen that the dead time between the gates pulses of one leg is successfully achieved, which is fixed to 4 μs.

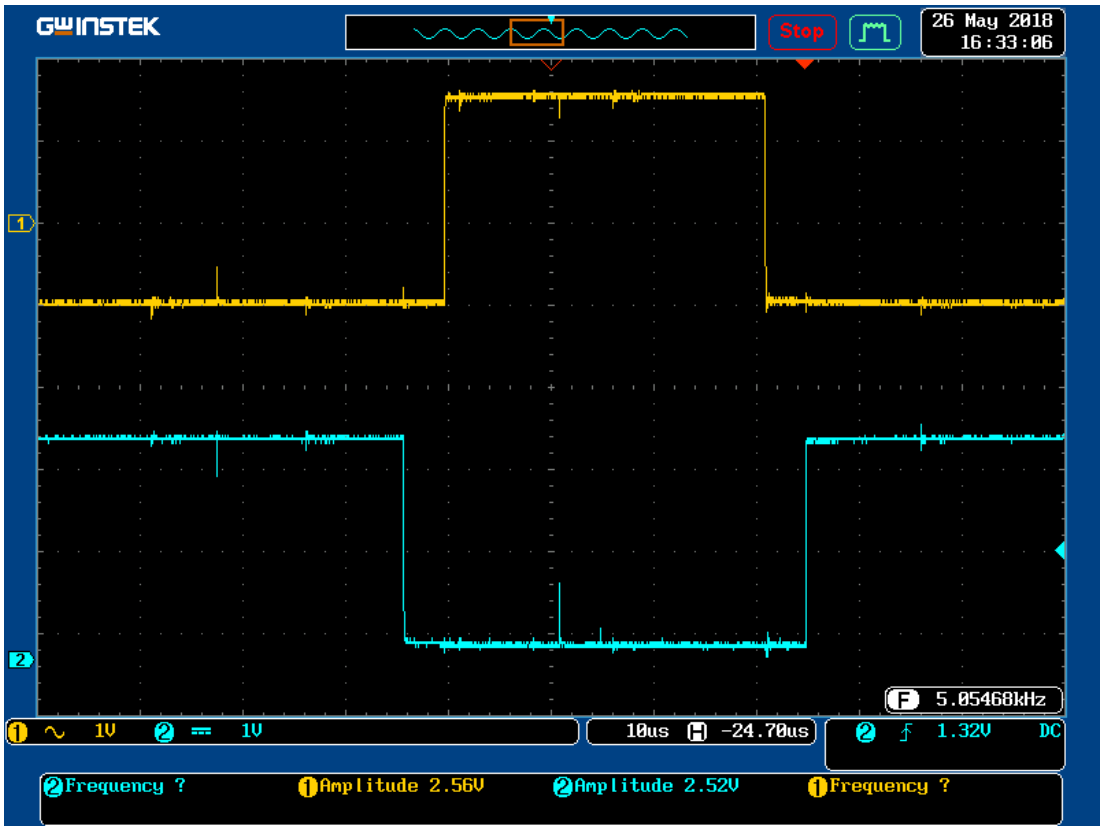


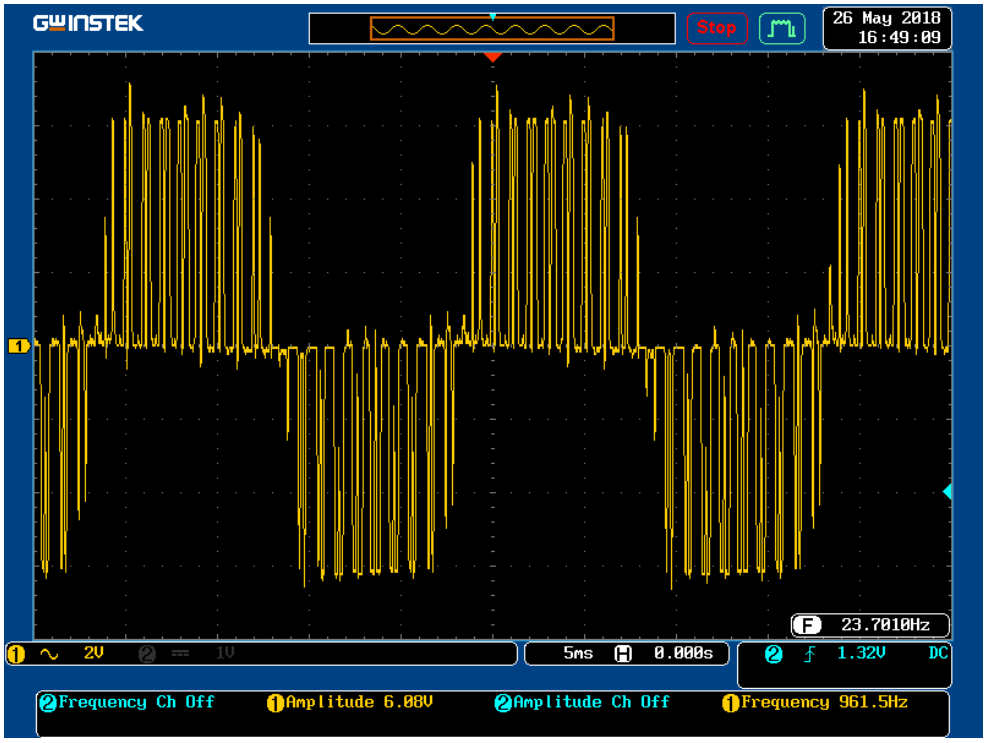
Figure (III. 13): Measured gate pulses of a switching device and its corresponding complementary

III.5.1. Balanced reference voltages condition

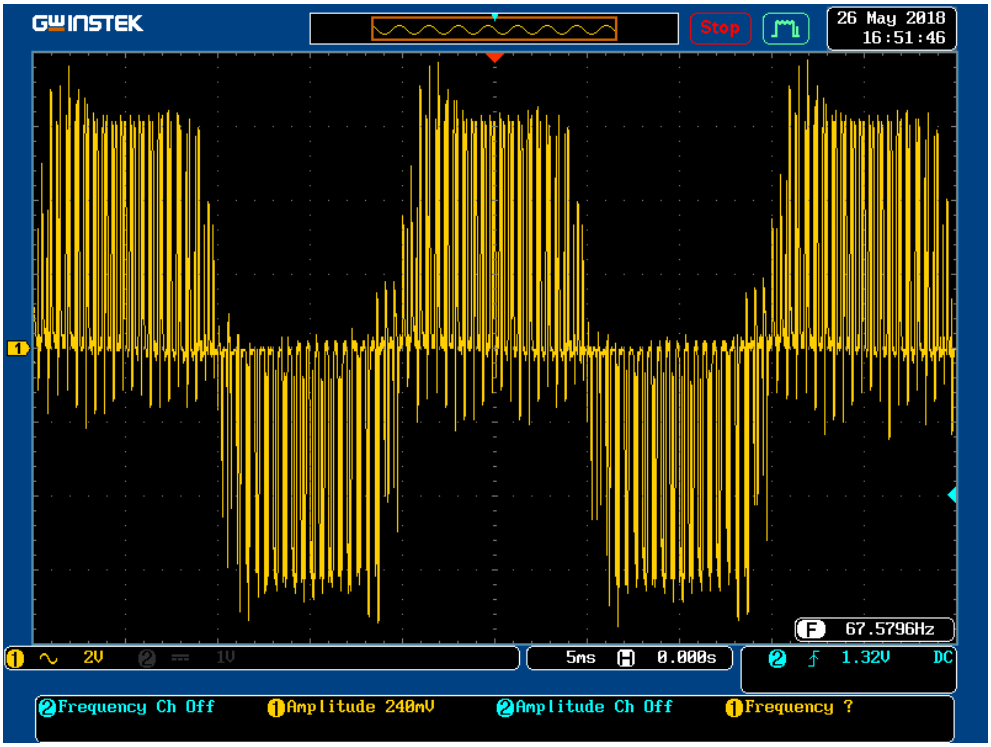
In this test, the three-phase reference voltages have the same amplitude of 30V, figures (III. 14) and (III. 15) show the waveforms of the output voltage of one phase (phase a) and load currents obtained under different switching frequencies (1, 2 and 5 kHz).

It is clear that the quality of the output voltage and load currents is enhanced when the switching frequency is increased.

(a)


GW INSTEK
Stop
26 May 2018
16:49:09
F 23.7010Hz
2V
1V
5ms
0.000s
1.32V
DC
Frequency Ch Off
Amplitude 6.08V
Amplitude Ch Off
Frequency 961.5Hz

(b)


GW INSTEK
Stop
26 May 2018
16:51:46
F 67.5796Hz
2V
1V
5ms
0.000s
1.32V
DC
Frequency Ch Off
Amplitude 240mV
Amplitude Ch Off
Frequency ?

(c)

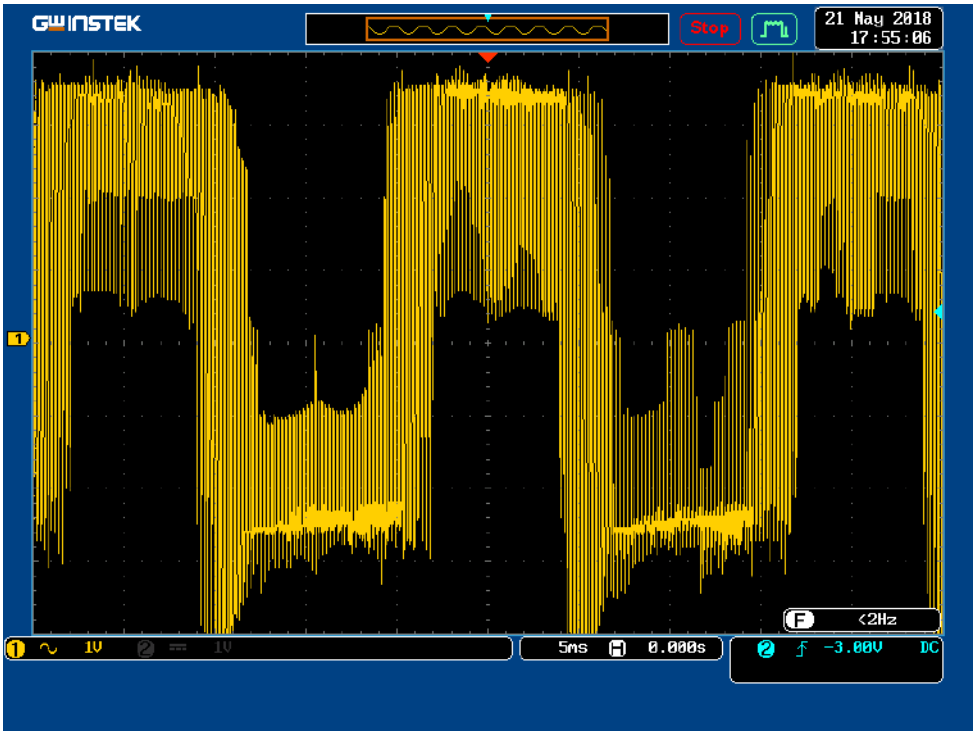
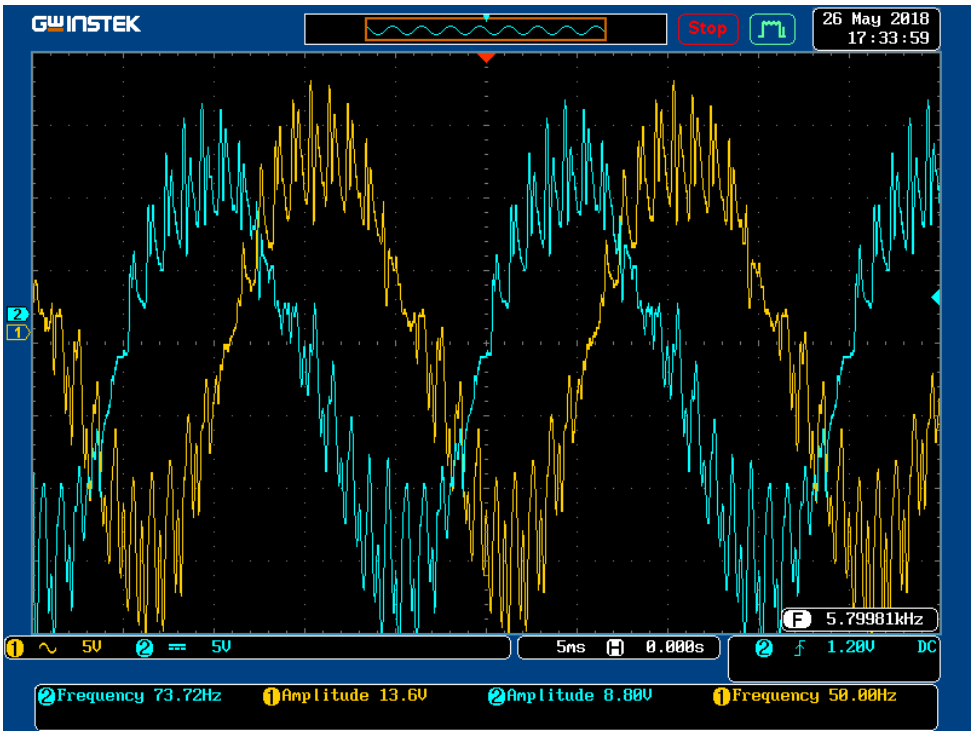
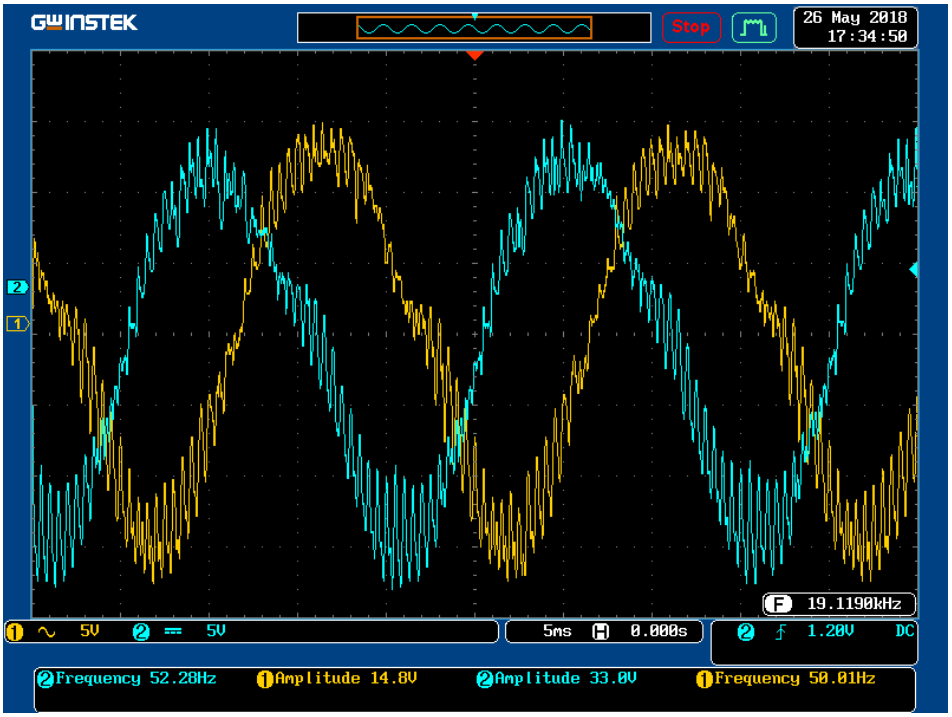


Figure (III.14): Experimental results of output voltage of the four-leg inverter under different switching frequencies, (a): 1 kHz, (b): 2 kHz, (c): 5 kHz

(a)



(b)



(c)

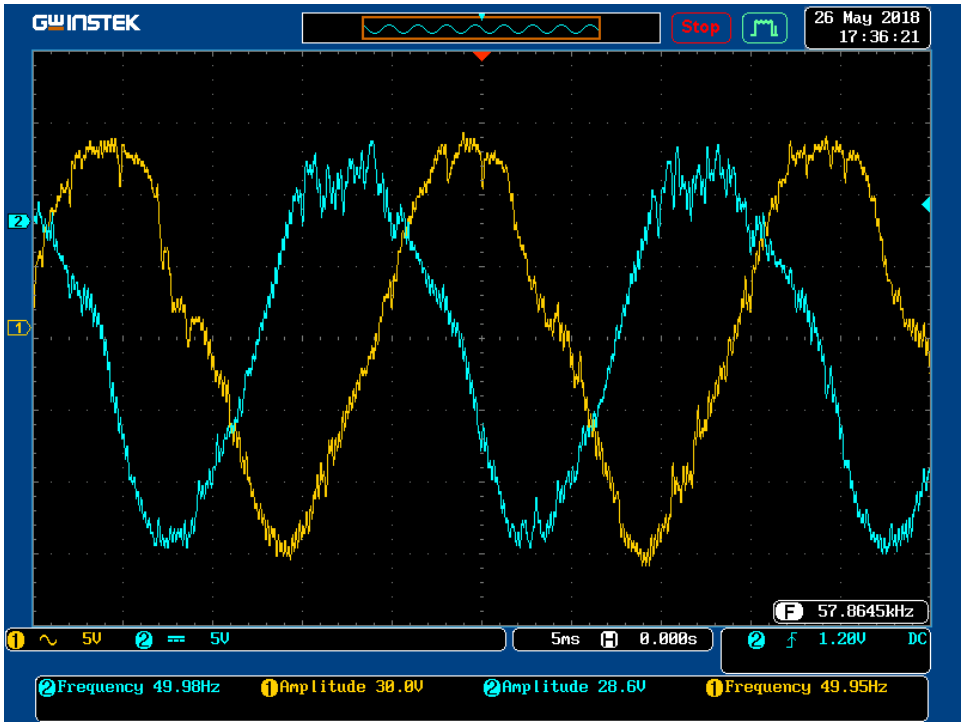


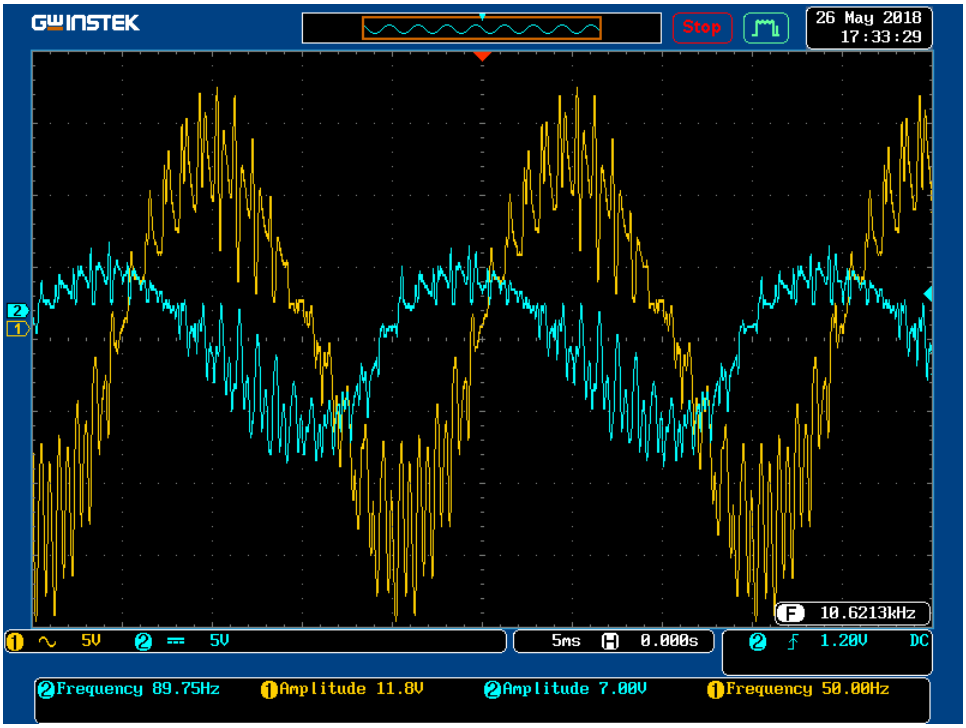
Figure (III.15): Experimental results of load current of phase (a) and phase (b) of the four-leg inverter under balanced reference voltages with different switching frequencies, (a): 1 kHz, (b): 2 kHz, (c): 5 kHz

III.5.2. Unbalanced reference voltages condition

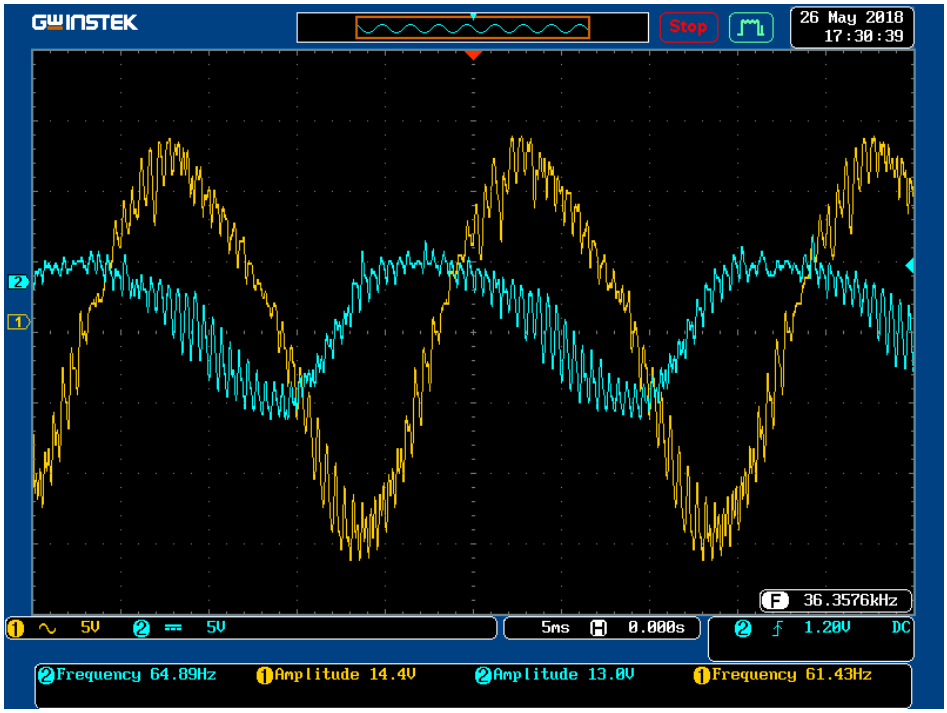
In this case, the amplitude of the reference voltage of phase (a) is reduced to 50% in order to induce an unbalanced reference voltage.

Figure (III. 16) presents the waveforms of the load currents of phase (a) and phase (b) under different switching frequencies (1, 2 and 5 kHz). As we can see, the amplitude of the load current of the phase (a) is reduced to 50% as compared with the phase (b). Because the amplitude of the reference voltage of the phase (a) is 50% of the amplitude of phases (b) and (c).

(a)



(b)



(c)

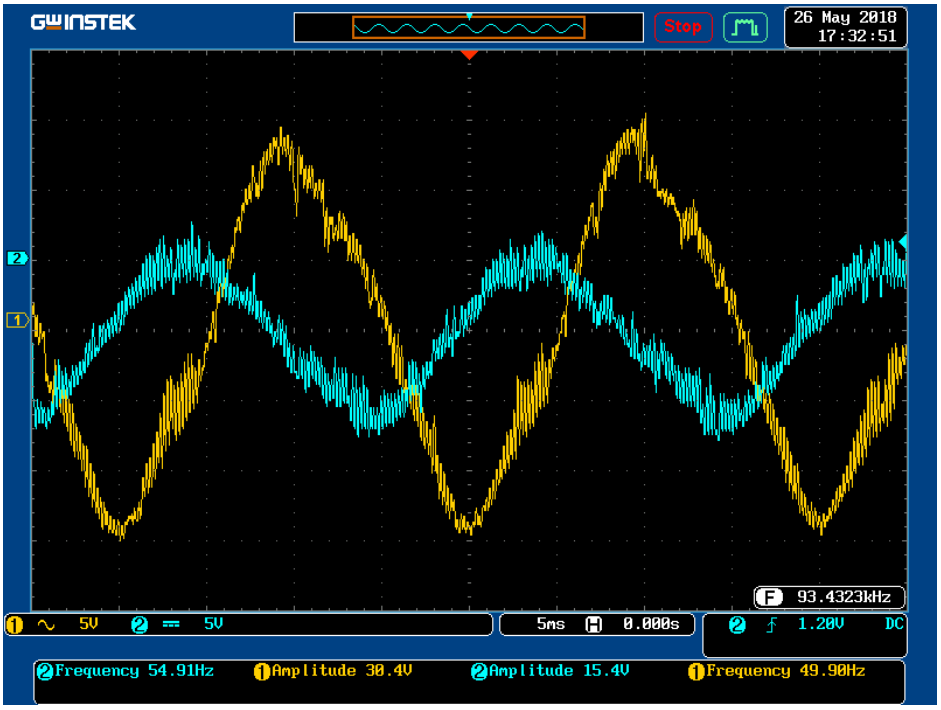


Figure (III.16): Experimental results of load current of phase (a) and phase (b) of the four-leg inverter under unbalanced reference voltages with different switching frequencies, (a): 1 kHz, (b): 2 kHz, (c): 5 kHz

III.6. Conclusion

In this chapter, a real-time approach for the implementation of the three-dimensional space vector modulation on four-leg inverters is introduced and described. The FPGA technology offer the ideal approach of designing PWM techniques for power electronics converters. The obtained experimental results are consistent with the analytical waveforms and demonstrate the feasibility and efficiency of the 3DSVM for three-phase four-leg inverters.

General conclusion

The three-phase four-leg inverter has been shown to be a solution for inverters operating in four-wire distribution systems.

In the first part of this work, the analysis and modeling of three-phase four-leg inverter is presented. According to the number switching states, the two-level four-leg inverter can provide sixteen switching voltages, which can be described using a graphical representation in three-dimensional space.

The three-dimensional space vector modulation is very suitable modulation technique for four-leg inverter. The 3DSVM algorithm has three main steps, which includes identification of the reference voltage vector location in the 3-D space, computing the switching vector duration times, and gate drive signal derivation. The simulation results demonstrate that the 3DSVM can control perfectly the four-leg voltage source inverters under balanced and unbalanced reference voltages conditions.
In other side, the implementation of 3DSVM for four-leg inverter is done using FPGA technology, which offer an ideal approach of designing PWM techniques for power electronics converters. The obtained experimental results are very consistent with the analytical waveforms, simulation results and demonstrate the feasibility and efficiency of the 3DSVM for three-phase four-leg inverters.

The following topics can be suggested for the future works:

- Apply the four-leg inverter to active filtering to enhance the power quality in four-wire system.
- Extension of 3DSVM to multilevel four-leg inverters,
- Using High-Level Synthesis Tools for Xilinx FPGA

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Appendix 1. A technical view of harmonics

Harmonics are currents or voltages with frequencies that are integer multiples of the fundamental power frequency. If the fundamental power frequency is 60 Hz, then the 2nd harmonic is 120 Hz, the 3rd is 180 Hz, etc. (see Figure 1). When harmonic frequencies are prevalent, electrical power panels and transformers become mechanically resonant to the magnetic fields generated by higher frequency harmonics. When this happens, the power panel or transformer vibrates and emits a buzzing sound for the different harmonic frequencies. Harmonic frequencies from the 3rd to the 25th are the most common range of frequencies measured in electrical distribution systems.

Appendix 2 THD definition

The total harmonic distortion (THD) of a signal is a measurement of the harmonic distortion present and is defined as the ratio of the sum of the powers of all harmonic components to the power of the fundamental. It provides an indication of the degree to which a voltage or current signal is distorted .THD is defined as

$$THD = \sqrt{\sum_{h=2}^{h=H}\left(\frac{Y_h}{Y_1}\right)^2} = \sqrt{\frac{Y_2^{\,2} + Y_3^{\,2} + Y_4^{\,2} .....}{Y_1^{\,2}}}$$

THD can exceed 1 and is generally expressed as a percentage.

Appendix 3 switching vectors coronations

Prisem 1	
Tetrahedron 1	$v_0(1110)\begin{pmatrix}0\\0\\\sqrt{3}v_{dc}\end{pmatrix}, v_1(1100)\begin{pmatrix}\frac{v_{dc}}{\sqrt{6}}\\\frac{v_{dc}}{\sqrt{2}}\\\frac{2v_{dc}}{\sqrt{3}}\end{pmatrix}, v_2(1000)\begin{pmatrix}\sqrt{\frac{2}{3}}v_{dc}\\0\\\frac{v_{dc}}{\sqrt{3}}\end{pmatrix}, v_3(0000,1111)\begin{pmatrix}0\\0\\0\end{pmatrix}$
Tetrahedron 2	$v_4(1101)\begin{pmatrix}\frac{v_{dc}}{\sqrt{6}}\\\frac{v_{dc}}{\sqrt{2}}\\\frac{-v_{dc}}{\sqrt{3}}\end{pmatrix}, v_1(1100)\begin{pmatrix}\frac{v_{dc}}{\sqrt{6}}\\\frac{v_{dc}}{\sqrt{2}}\\\frac{2v_{dc}}{\sqrt{3}}\end{pmatrix}, v_2(1000)\begin{pmatrix}\sqrt{\frac{2}{3}}v_{dc}\\0\\\frac{v_{dc}}{\sqrt{3}}\end{pmatrix}, v_3(0000,1111)\begin{pmatrix}0\\0\\0\end{pmatrix}$
Tetrahedron 3	$v_4(1101)\begin{pmatrix}\frac{v_{dc}}{\sqrt{6}}\\\frac{v_{dc}}{\sqrt{2}}\\\frac{-v_{dc}}{\sqrt{3}}\end{pmatrix}, v_5(1001)\begin{pmatrix}\sqrt{\frac{2}{3}}v_{dc}\\0\\\frac{-2v_{dc}}{\sqrt{3}}\end{pmatrix}, v_2(1000)\begin{pmatrix}\sqrt{\frac{2}{3}}v_{dc}\\0\\\frac{v_{dc}}{\sqrt{3}}\end{pmatrix}, v_3(0000,1111)\begin{pmatrix}0\\0\\0\end{pmatrix}$
Tetrahedron 4	$v_4(1101)\begin{pmatrix}\frac{v_{dc}}{\sqrt{6}}\\\frac{v_{dc}}{\sqrt{2}}\\\frac{-v_{dc}}{\sqrt{3}}\end{pmatrix}, v_5(1001)\begin{pmatrix}\sqrt{\frac{2}{3}}v_{dc}\\0\\\frac{-2v_{dc}}{\sqrt{3}}\end{pmatrix}, v_6(0001)\begin{pmatrix}0\\0\\-\sqrt{3}v_{dc}\end{pmatrix}, v_3(0000,1111)\begin{pmatrix}0\\0\\0\end{pmatrix}$

Prisem 2	
Tetrahedron 1	$v_0(1110)\begin{pmatrix}0\\0\\\sqrt{3}v_{dc}\end{pmatrix}, v_1(1100)\begin{pmatrix}\frac{v_{dc}}{\sqrt{6}}\\\frac{v_{dc}}{\sqrt{2}}\\\frac{2v_{dc}}{\sqrt{3}}\end{pmatrix}, v_7(0100)\begin{pmatrix}\frac{-v_{dc}}{\sqrt{6}}\\\frac{v_{dc}}{\sqrt{2}}\\\frac{v_{dc}}{\sqrt{3}}\end{pmatrix}, v_3(0000,1111)\begin{pmatrix}0\\0\\0\end{pmatrix}$
Tetrahedron 2	$v_4(1101)\begin{pmatrix}\frac{v_{dc}}{\sqrt{6}}\\\frac{v_{dc}}{\sqrt{2}}\\\frac{-v_{dc}}{\sqrt{3}}\end{pmatrix}, v_1(1100)\begin{pmatrix}\frac{v_{dc}}{\sqrt{6}}\\\frac{v_{dc}}{\sqrt{2}}\\\frac{2v_{dc}}{\sqrt{3}}\end{pmatrix}, v_7(0100)\begin{pmatrix}\frac{-v_{dc}}{\sqrt{6}}\\\frac{v_{dc}}{\sqrt{2}}\\\frac{v_{dc}}{\sqrt{3}}\end{pmatrix}, v_3(0000,1111)\begin{pmatrix}0\\0\\0\end{pmatrix}$
Tetrahedron 3	$v_4(1101)\begin{pmatrix}\frac{v_{dc}}{\sqrt{6}}\\\frac{v_{dc}}{\sqrt{2}}\\\frac{-v_{dc}}{\sqrt{3}}\end{pmatrix}, v_8(0101)\begin{pmatrix}\frac{-v_{dc}}{\sqrt{6}}\\\frac{v_{dc}}{\sqrt{2}}\\\frac{-2v_{dc}}{\sqrt{3}}\end{pmatrix}, v_7(0100)\begin{pmatrix}\frac{-v_{dc}}{\sqrt{6}}\\\frac{v_{dc}}{\sqrt{2}}\\\frac{v_{dc}}{\sqrt{3}}\end{pmatrix}, v_3(0000,1111)\begin{pmatrix}0\\0\\0\end{pmatrix}$
Tetrahedron 4	$v_5(1101)\begin{pmatrix}\frac{v_{dc}}{\sqrt{6}}\\\frac{v_{dc}}{\sqrt{2}}\\\frac{-v_{dc}}{\sqrt{3}}\end{pmatrix}, v_1(1100)\begin{pmatrix}\frac{v_{dc}}{\sqrt{6}}\\\frac{v_{dc}}{\sqrt{2}}\\\frac{2v_{dc}}{\sqrt{3}}\end{pmatrix}, v_8(0100)\begin{pmatrix}\frac{-v_{dc}}{\sqrt{6}}\\\frac{v_{dc}}{\sqrt{2}}\\\frac{v_{dc}}{\sqrt{3}}\end{pmatrix}, v_3(0000,1111)\begin{pmatrix}0\\0\\0\end{pmatrix}$

Prisem 3	
Tetrahedron 1	$v_0(1110)\begin{pmatrix}0\\0\\\sqrt{3}v_{dc}\end{pmatrix}, v_9(0110)\begin{pmatrix}\sqrt{\frac{2}{3}}v_{dc}\\0\\\frac{2v_{dc}}{\sqrt{3}}\end{pmatrix}, v_7(0100)\begin{pmatrix}\frac{-v_{dc}}{\sqrt{6}}\\\frac{v_{dc}}{\sqrt{2}}\\\frac{v_{dc}}{\sqrt{3}}\end{pmatrix}, v_3(0000,1111)\begin{pmatrix}0\\0\\0\end{pmatrix}$
Tetrahedron 2	$v_8(0101)\begin{pmatrix}\frac{v_{dc}}{\sqrt{6}}\\\frac{v_{dc}}{\sqrt{2}}\\\frac{-v_{dc}}{\sqrt{3}}\end{pmatrix}, v_9(0110)\begin{pmatrix}\sqrt{\frac{2}{3}}v_{dc}\\0\\\frac{2v_{dc}}{\sqrt{3}}\end{pmatrix}, v_7(0100)\begin{pmatrix}\frac{-v_{dc}}{\sqrt{6}}\\\frac{v_{dc}}{\sqrt{2}}\\\frac{v_{dc}}{\sqrt{3}}\end{pmatrix}, v_3(0000,1111)\begin{pmatrix}0\\0\\0\end{pmatrix}$
Tetrahedron 3	$v_8(0101)\begin{pmatrix}\frac{v_{dc}}{\sqrt{6}}\\\frac{v_{dc}}{\sqrt{2}}\\\frac{-v_{dc}}{\sqrt{3}}\end{pmatrix}, v_9(0110)\begin{pmatrix}\sqrt{\frac{2}{3}}v_{dc}\\0\\\frac{2v_{dc}}{\sqrt{3}}\end{pmatrix}, v_{10}(0111)\begin{pmatrix}\sqrt{\frac{2}{3}}v_{dc}\\0\\\frac{-v_{dc}}{\sqrt{3}}\end{pmatrix}, v_3(0000,1111)\begin{pmatrix}0\\0\\0\end{pmatrix}$
Tetrahedron 4	$v_8(0101)\begin{pmatrix}\frac{v_{dc}}{\sqrt{6}}\\\frac{v_{dc}}{\sqrt{2}}\\\frac{-v_{dc}}{\sqrt{3}}\end{pmatrix}, v_6(0001)\begin{pmatrix}0\\0\\-\sqrt{3}v_{dc}\end{pmatrix}, v_{10}(0111)\begin{pmatrix}\sqrt{\frac{2}{3}}v_{dc}\\0\\\frac{-v_{dc}}{\sqrt{3}}\end{pmatrix}, v_3(0000,1111)\begin{pmatrix}0\\0\\0\end{pmatrix}$

Prisem 4	
Tetrahedron 1	$v_0(1110)\begin{pmatrix}0\\0\\\sqrt{3}v_{dc}\end{pmatrix}, v_9(0110)\begin{pmatrix}\sqrt{\frac{2}{3}}v_{dc}\\0\\\frac{2v_{dc}}{\sqrt{3}}\end{pmatrix}, v_{11}(0010)\begin{pmatrix}\frac{-v_{dc}}{\sqrt{6}}\\\frac{-v_{dc}}{\sqrt{2}}\\\frac{v_{dc}}{\sqrt{3}}\end{pmatrix}, v_3(0000,1111)\begin{pmatrix}0\\0\\0\end{pmatrix}$
Tetrahedron 2	$v_{10}(0111)\begin{pmatrix}\sqrt{\frac{2}{3}}v_{dc}\\0\\\frac{-v_{dc}}{\sqrt{3}}\end{pmatrix}, v_9(0110)\begin{pmatrix}\sqrt{\frac{2}{3}}v_{dc}\\0\\\frac{2v_{dc}}{\sqrt{3}}\end{pmatrix}, v_{11}(0010)\begin{pmatrix}\frac{-v_{dc}}{\sqrt{6}}\\\frac{-v_{dc}}{\sqrt{2}}\\\frac{v_{dc}}{\sqrt{3}}\end{pmatrix}, v_3(0000,1111)\begin{pmatrix}0\\0\\0\end{pmatrix}$
Tetrahedron 3	$v_{10}(0111)\begin{pmatrix}\sqrt{\frac{2}{3}}v_{dc}\\0\\\frac{-v_{dc}}{\sqrt{3}}\end{pmatrix}, v_{12}(0011)\begin{pmatrix}\frac{-v_{dc}}{\sqrt{6}}\\\frac{-v_{dc}}{\sqrt{2}}\\\frac{-2v_{dc}}{\sqrt{3}}\end{pmatrix}, v_{11}(0010)\begin{pmatrix}\frac{-v_{dc}}{\sqrt{6}}\\\frac{-v_{dc}}{\sqrt{2}}\\\frac{v_{dc}}{\sqrt{3}}\end{pmatrix}, v_3(0000,1111)\begin{pmatrix}0\\0\\0\end{pmatrix}$
Tetrahedron 4	$v_{10}(0111)\begin{pmatrix}\sqrt{\frac{2}{3}}v_{dc}\\0\\\frac{-v_{dc}}{\sqrt{3}}\end{pmatrix}, v_{12}(0011)\begin{pmatrix}\frac{-v_{dc}}{\sqrt{6}}\\\frac{-v_{dc}}{\sqrt{2}}\\\frac{-2v_{dc}}{\sqrt{3}}\end{pmatrix}, v_6(0001)\begin{pmatrix}0\\0\\-\sqrt{3}v_{dc}\end{pmatrix}, v_3(0000,1111)\begin{pmatrix}0\\0\\0\end{pmatrix}$

Prisem 5	
Tetrahedron 1	$v_0(1110)\begin{pmatrix}0\\0\\\sqrt{3}v_{dc}\end{pmatrix}, v_{13}(1010)\begin{pmatrix}\frac{v_{dc}}{\sqrt{6}}\\\frac{-v_{dc}}{\sqrt{2}}\\\frac{2v_{dc}}{\sqrt{3}}\end{pmatrix}, v_{11}(0010)\begin{pmatrix}\frac{-v_{dc}}{\sqrt{6}}\\\frac{-v_{dc}}{\sqrt{2}}\\\frac{v_{dc}}{\sqrt{3}}\end{pmatrix}, v_3(0000,1111)\begin{pmatrix}0\\0\\0\end{pmatrix}$
Tetrahedron 2	$v_{14}(1011)\begin{pmatrix}\frac{v_{dc}}{\sqrt{6}}\\\frac{-v_{dc}}{\sqrt{2}}\\\frac{-v_{dc}}{\sqrt{3}}\end{pmatrix}, v_{13}(1010)\begin{pmatrix}\frac{v_{dc}}{\sqrt{6}}\\\frac{-v_{dc}}{\sqrt{2}}\\\frac{2v_{dc}}{\sqrt{3}}\end{pmatrix}, v_{11}(0010)\begin{pmatrix}\frac{-v_{dc}}{\sqrt{6}}\\\frac{-v_{dc}}{\sqrt{2}}\\\frac{v_{dc}}{\sqrt{3}}\end{pmatrix}, v_3(0000,1111)\begin{pmatrix}0\\0\\0\end{pmatrix}$
Tetrahedron 3	$v_{14}(1011)\begin{pmatrix}\frac{v_{dc}}{\sqrt{6}}\\\frac{-v_{dc}}{\sqrt{2}}\\\frac{-v_{dc}}{\sqrt{3}}\end{pmatrix}, v_{12}(0011)\begin{pmatrix}\frac{-v_{dc}}{\sqrt{6}}\\\frac{-v_{dc}}{\sqrt{2}}\\\frac{-2v_{dc}}{\sqrt{3}}\end{pmatrix}, v_{11}(0010)\begin{pmatrix}\frac{-v_{dc}}{\sqrt{6}}\\\frac{-v_{dc}}{\sqrt{2}}\\\frac{v_{dc}}{\sqrt{3}}\end{pmatrix}, v_3(0000,1111)\begin{pmatrix}0\\0\\0\end{pmatrix}$
Tetrahedron 4	$v_{14}(1011)\begin{pmatrix}\frac{v_{dc}}{\sqrt{6}}\\\frac{-v_{dc}}{\sqrt{2}}\\\frac{-v_{dc}}{\sqrt{3}}\end{pmatrix}, v_{12}(0011)\begin{pmatrix}\frac{-v_{dc}}{\sqrt{6}}\\\frac{-v_{dc}}{\sqrt{2}}\\\frac{-2v_{dc}}{\sqrt{3}}\end{pmatrix}, v_6(0001)\begin{pmatrix}0\\0\\-\sqrt{3}v_{dc}\end{pmatrix}, v_3(0000,1111)\begin{pmatrix}0\\0\\0\end{pmatrix}$

Prisem 6	
Tetrahedron 1	$v_0(1110)\begin{pmatrix}0\\0\\\sqrt{3}v_{dc}\end{pmatrix}, v_{13}(1010)\begin{pmatrix}\frac{v_{dc}}{\sqrt{6}}\\\frac{-v_{dc}}{\sqrt{2}}\\\frac{2v_{dc}}{\sqrt{3}}\end{pmatrix}, v_2(1000)\begin{pmatrix}\sqrt{\frac{2}{3}}v_{dc}\\0\\\frac{v_{dc}}{\sqrt{3}}\end{pmatrix}, v_3(0000,1111)\begin{pmatrix}0\\0\\0\end{pmatrix}$
Tetrahedron 2	$v_{15}(1001)\begin{pmatrix}\sqrt{\frac{2}{3}}v_{dc}\\0\\\frac{-2v_{dc}}{\sqrt{3}}\end{pmatrix}, v_{13}(1010)\begin{pmatrix}\frac{v_{dc}}{\sqrt{6}}\\\frac{-v_{dc}}{\sqrt{2}}\\\frac{2v_{dc}}{\sqrt{3}}\end{pmatrix}, v_2(1000)\begin{pmatrix}\sqrt{\frac{2}{3}}v_{dc}\\0\\\frac{v_{dc}}{\sqrt{3}}\end{pmatrix}, v_3(0000,1111)\begin{pmatrix}0\\0\\0\end{pmatrix}$
Tetrahedron 3	$v_{15}(1001)\begin{pmatrix}\sqrt{\frac{2}{3}}v_{dc}\\0\\\frac{-2v_{dc}}{\sqrt{3}}\end{pmatrix}, v_{13}(1010)\begin{pmatrix}\frac{v_{dc}}{\sqrt{6}}\\\frac{-v_{dc}}{\sqrt{2}}\\\frac{2v_{dc}}{\sqrt{3}}\end{pmatrix}, v_{14}(1011)\begin{pmatrix}\frac{v_{dc}}{\sqrt{6}}\\\frac{-v_{dc}}{\sqrt{2}}\\\frac{-v_{dc}}{\sqrt{3}}\end{pmatrix}, v_3(0000,1111)\begin{pmatrix}0\\0\\0\end{pmatrix}$
Tetrahedron 4	$v_{15}(1001)\begin{pmatrix}\sqrt{\frac{2}{3}}v_{dc}\\0\\\frac{-2v_{dc}}{\sqrt{3}}\end{pmatrix}, v_{14}(1011)\begin{pmatrix}\frac{v_{dc}}{\sqrt{6}}\\\frac{-v_{dc}}{\sqrt{2}}\\\frac{-v_{dc}}{\sqrt{3}}\end{pmatrix}, v_6(0001)\begin{pmatrix}0\\0\\-\sqrt{3}v_{dc}\end{pmatrix}, v_3(0000,1111)\begin{pmatrix}0\\0\\0\end{pmatrix}$

Appendix 4 Time intervals with tetrahedron locations

Prism2	On duration time intervals	Condition of localisation
Tetrahedron 1	$\begin{bmatrix} t_1 \\ t_2 \\ t_3 \end{bmatrix} = \begin{bmatrix} -\frac{\sqrt{6}}{6} & -\frac{\sqrt{2}}{2} & \frac{\sqrt{3}}{3} \\ \frac{\sqrt{6}}{2} & \frac{\sqrt{2}}{2} & 0 \\ \sqrt{3} & \frac{\sqrt{2}}{2} & 0 \end{bmatrix} \begin{bmatrix} v_\alpha^* T_s \\ v_\beta^* T_s \\ v_o^* T_s \end{bmatrix} \times \frac{1}{v_{dc}}$ $T_4 = T_s - T_1 - T_2 - T_3$	$v_\gamma \le \frac{1}{\sqrt{2}} v_\alpha - \sqrt{\frac{3}{2}} v_\beta + \sqrt{3} v_{dc}$ $v_\gamma > \frac{v_\alpha}{\sqrt{2}} + \sqrt{\frac{3}{2}} v_\beta$
Tetrahedron 2	$\begin{bmatrix} t_1 \\ t_2 \\ t_3 \end{bmatrix} = \begin{bmatrix} \frac{\sqrt{6}}{3} & 0 & \frac{\sqrt{3}}{3} \\ -\frac{\sqrt{6}}{2} & \frac{\sqrt{2}}{2} & 0 \\ \frac{\sqrt{6}}{6} & \frac{\sqrt{2}}{2} & -\frac{\sqrt{3}}{3} \end{bmatrix} \begin{bmatrix} v_\alpha^* T_s \\ v_\beta^* T_s \\ v_o^* T_s \end{bmatrix} \times \frac{1}{v_{dc}}$ $T_4 = T_s - T_1 - T_2 - T_3$	$v_\gamma \le \frac{v_\alpha}{\sqrt{2}} + \sqrt{\frac{3}{2}} v_\beta$ $v_\gamma > -\sqrt{2} v_\alpha$
Tetrahedron 3	$\begin{bmatrix} t_1 \\ t_2 \\ t_3 \end{bmatrix} = \begin{bmatrix} -\frac{\sqrt{6}}{6} & \frac{\sqrt{2}}{2} & -\frac{\sqrt{3}}{3} \\ \frac{\sqrt{6}}{2} & \frac{\sqrt{2}}{2} & 0 \\ -\frac{\sqrt{6}}{3} & 0 & -\frac{\sqrt{3}}{3} \end{bmatrix} \begin{bmatrix} v_\alpha^* T_s \\ v_\beta^* T_s \\ v_o^* T_s \end{bmatrix} \times \frac{1}{v_{dc}}$ $T_4 = T_s - T_1 - T_2 - T_3$	$v_\gamma \le -\sqrt{2} v_\alpha$ $v_\gamma > \frac{1}{\sqrt{2}} v_\alpha - \sqrt{\frac{3}{2}} v_\beta$
Tetrahedron 4	$\begin{bmatrix} t_1 \\ t_2 \\ t_3 \end{bmatrix} = \begin{bmatrix} \frac{\sqrt{6}}{2} & \frac{\sqrt{2}}{2} & 0 \\ \frac{\sqrt{6}}{2} & \frac{\sqrt{2}}{2} & 0 \\ \frac{\sqrt{6}}{6} & -\frac{\sqrt{2}}{2} & -\frac{\sqrt{3}}{3} \end{bmatrix} \begin{bmatrix} v_\alpha^* T_s \\ v_\beta^* T_s \\ v_o^* T_s \end{bmatrix} \times \frac{1}{v_{dc}}$ $T_4 = T_s - T_1 - T_2 - T_3$	$v_\gamma \le \frac{1}{\sqrt{2}} v_\alpha - \sqrt{\frac{3}{2}} v_\beta$ $v_\gamma \le \frac{1}{\sqrt{2}} v_\alpha + \sqrt{\frac{3}{2}} v_\beta - \sqrt{3} v_{dc}$

Prism3	On duration time intervals	Condition of localisation
Tetrahedron 1	$\begin{bmatrix} t_1 \\ t_2 \\ t_3 \end{bmatrix} = \begin{bmatrix} \frac{\sqrt{6}}{3} & 0 & \frac{\sqrt{3}}{3} \\ -\frac{\sqrt{6}}{2} & -\frac{\sqrt{2}}{2} & 0 \\ 0 & \sqrt{2} & 0 \end{bmatrix} \begin{bmatrix} v_\alpha^* T_s \\ v_\beta^* T_s \\ v_o^* T_s \end{bmatrix} \times \frac{1}{V_{dc}}$ $T_4 = T_s - T_1 - T_2 - T_3$	$v_\gamma \le \frac{1}{\sqrt{2}} v_\alpha - \sqrt{\frac{3}{2}} v_\beta + \sqrt{3} v_{dc}$ $v_\gamma > -\sqrt{2} v_\alpha$
Tetrahedron 2	$\begin{bmatrix} t_1 \\ t_2 \\ t_3 \end{bmatrix} = \begin{bmatrix} -\frac{\sqrt{6}}{6} & -\frac{\sqrt{2}}{2} & \frac{\sqrt{3}}{3} \\ 0 & \sqrt{2} & 0 \\ \frac{\sqrt{6}}{3} & 0 & -\frac{\sqrt{3}}{3} \end{bmatrix} \begin{bmatrix} v_\alpha^* T_s \\ v_\beta^* T_s \\ v_o^* T_s \end{bmatrix} \times \frac{1}{V_{dc}}$ $T_4 = T_s - T_1 - T_2 - T_3$	$v_\gamma \le -\sqrt{2} v_\alpha$ $v_\gamma > \sqrt{2} v_\alpha + \sqrt{\frac{3}{2}} v_\beta$
Tetrahedron 3	$\begin{bmatrix} t_1 \\ t_2 \\ t_3 \end{bmatrix} = \begin{bmatrix} -\frac{\sqrt{6}}{6} & \frac{\sqrt{2}}{2} & \frac{\sqrt{3}}{3} \\ -\frac{\sqrt{6}}{2} & -\frac{\sqrt{2}}{2} & 0 \\ \frac{\sqrt{6}}{6} & \frac{\sqrt{2}}{2} & -\frac{\sqrt{3}}{3} \end{bmatrix} \begin{bmatrix} v_\alpha^* T_s \\ v_\beta^* T_s \\ v_o^* T_s \end{bmatrix} \times \frac{1}{V_{dc}}$ $T_4 = T_s - T_1 - T_2 - T_3$	$v_\gamma \le \sqrt{2} v_\alpha + \sqrt{\frac{3}{2}} v_\beta$ $v_\gamma > \frac{1}{\sqrt{2}} v_\alpha - \sqrt{\frac{3}{2}} v_\beta$
Tetrahedron 4	$\begin{bmatrix} t_1 \\ t_2 \\ t_3 \end{bmatrix} = \begin{bmatrix} -\frac{\sqrt{6}}{2} & -\frac{\sqrt{2}}{2} & 0 \\ 0 & \frac{\sqrt{2}}{2} & 0 \\ \frac{\sqrt{6}}{6} & -\frac{\sqrt{3}}{3} & -\frac{\sqrt{3}}{3} \end{bmatrix} \begin{bmatrix} v_\alpha^* T_s \\ v_\beta^* T_s \\ v_o^* T_s \end{bmatrix} \times \frac{1}{V_{dc}}$ $T_4 = T_s - T_1 - T_2 - T_3$	$v_\gamma \le \frac{1}{\sqrt{2}} v_\alpha - \sqrt{\frac{3}{2}} v_\beta$ $v_\gamma > -\sqrt{2} v_\alpha - \sqrt{3} v_{dc}$

prism4	On duration time inter vals	Condition of localisation
Tetrahedron 1	$\begin{bmatrix} t_1 \\ t_2 \\ t_3 \end{bmatrix} = \begin{bmatrix} \frac{\sqrt{6}}{3} & 0 & \frac{\sqrt{3}}{3} \\ -\frac{\sqrt{6}}{2} & \frac{\sqrt{2}}{2} & 0 \\ \frac{\sqrt{6}}{6} & -\sqrt{2} & 0 \end{bmatrix} \begin{bmatrix} v_\alpha^* T_s \\ v_\beta^* T_s \\ v_o^* T_s \end{bmatrix} \times \frac{1}{v_{dc}}$ $T_4 = T_s - T_1 - T_2 - T_3$	$v_\gamma \le \frac{v_a}{\sqrt{2}} + \sqrt{\frac{3}{2}} v_\beta + \sqrt{3} v_{dc}$ $v_\gamma > -\sqrt{2} v_a$
Tetrahedron 2	$\begin{bmatrix} t_1 \\ t_2 \\ t_3 \end{bmatrix} = \begin{bmatrix} \frac{-\sqrt{6}}{6} & -\frac{\sqrt{2}}{2} & -\frac{\sqrt{3}}{3} \\ -\frac{\sqrt{6}}{2} & \frac{\sqrt{2}}{2} & 0 \\ \frac{\sqrt{6}}{6} & -\frac{\sqrt{2}}{2} & -\frac{\sqrt{3}}{3} \end{bmatrix} \begin{bmatrix} v_\alpha^* T_s \\ v_\beta^* T_s \\ v_o^* T_s \end{bmatrix} \times \frac{1}{v_{dc}}$ $T_4 = T_s - T_1 - T_2 - T_3$	$v_\gamma \le -\sqrt{2} v_a$ $v_\gamma > \frac{v_a}{\sqrt{2}} - \sqrt{\frac{3}{2}} v_\beta$
Tetrahedron 3	$\begin{bmatrix} t_1 \\ t_2 \\ t_3 \end{bmatrix} = \begin{bmatrix} -\frac{\sqrt{6}}{6} & \frac{\sqrt{2}}{2} & \frac{\sqrt{3}}{3} \\ -\frac{\sqrt{6}}{2} & \frac{\sqrt{2}}{2} & 0 \\ \frac{\sqrt{6}}{6} & -\frac{\sqrt{2}}{2} & -\frac{\sqrt{3}}{3} \end{bmatrix} \begin{bmatrix} v_\alpha^* T_s \\ v_\beta^* T_s \\ v_o^* T_s \end{bmatrix} \times \frac{1}{v_{dc}}$ $T_4 = T_s - T_1 - T_2 - T_3$	$v_\gamma \le \frac{v_a}{\sqrt{2}} - \sqrt{\frac{3}{2}} v_\beta$ $v_\gamma > \frac{v_a}{\sqrt{2}} + \sqrt{\frac{3}{2}} v_\beta$
Tetrahedron 4	$\begin{bmatrix} t_1 \\ t_2 \\ t_3 \end{bmatrix} = \begin{bmatrix} -\frac{\sqrt{6}}{2} & -\frac{\sqrt{2}}{2} & 0 \\ 0 & -\frac{\sqrt{2}}{2} & 0 \\ -\frac{\sqrt{6}}{6} & -\frac{\sqrt{2}}{2} & -\frac{\sqrt{3}}{3} \end{bmatrix} \begin{bmatrix} v_\alpha^* T_s \\ v_\beta^* T_s \\ v_o^* T_s \end{bmatrix} \times \frac{1}{v_{dc}}$ $T_4 = T_s - T_1 - T_2 - T_3$	$v_\gamma \le \frac{v_a}{\sqrt{2}} + \sqrt{\frac{3}{2}} v_\beta$ $v_\gamma > -\sqrt{2} v_a - \sqrt{3} v_{dc}$

Prism 5	On duration time inter vals	Condition of localisation
Tetrahedron 1	$\begin{bmatrix} t_1 \\ t_2 \\ t_3 \end{bmatrix} = \begin{bmatrix} -\frac{\sqrt{6}}{6} & \frac{\sqrt{2}}{2} & \frac{\sqrt{3}}{3} \\ \frac{\sqrt{6}}{2} & -\frac{\sqrt{2}}{2} & 0 \\ -\frac{\sqrt{6}}{2} & -\frac{\sqrt{2}}{2} & 0 \end{bmatrix} \begin{bmatrix} v_\alpha^* T_s \\ v_\beta^* T_s \\ v_o^* T_s \end{bmatrix} \times \frac{1}{v_{dc}}$ $T_4 = T_s - T_1 - T_2 - T_3$	$v_\gamma \le \frac{v_a}{\sqrt{2}} + \sqrt{\frac{3}{2}} v_\beta + \sqrt{3} v_{dc}$ $v_\gamma > \frac{v_a}{\sqrt{2}} - \sqrt{\frac{3}{2}} v_\beta$
Tetrahedron 2	$\begin{bmatrix} t_1 \\ t_2 \\ t_3 \end{bmatrix} = \begin{bmatrix} \frac{\sqrt{6}}{3} & 0 & \frac{\sqrt{3}}{3} \\ -\frac{\sqrt{6}}{2} & -\frac{\sqrt{2}}{2} & 0 \\ -\frac{\sqrt{6}}{6} & -\frac{\sqrt{2}}{2} & -\frac{\sqrt{3}}{3} \end{bmatrix} \begin{bmatrix} v_\alpha^* T_s \\ v_\beta^* T_s \\ v_o^* T_s \end{bmatrix} \times \frac{1}{v_{dc}}$ $T_4 = T_s - T_1 - T_2 - T_3$	$v_\gamma \le \frac{v_a}{\sqrt{2}} - \sqrt{\frac{3}{2}} v_\beta$ $v_\gamma > -\sqrt{2} v_\alpha$
Tetrahedron 3	$\begin{bmatrix} t_1 \\ t_2 \\ t_3 \end{bmatrix} = \begin{bmatrix} -\frac{\sqrt{6}}{6} & -\frac{\sqrt{2}}{2} & \frac{\sqrt{3}}{3} \\ \frac{\sqrt{6}}{2} & -\frac{\sqrt{2}}{2} & 0 \\ -\frac{\sqrt{6}}{3} & 0 & -\frac{\sqrt{3}}{3} \end{bmatrix} \begin{bmatrix} v_\alpha^* T_s \\ v_\beta^* T_s \\ v_o^* T_s \end{bmatrix} \times \frac{1}{v_{dc}}$ $T_4 = T_s - T_1 - T_2 - T_3$	$v_\gamma \le -\sqrt{2} v_\alpha$ $v_\gamma > \frac{v_a}{\sqrt{2}} + \sqrt{\frac{3}{2}} v_\beta$
Tetrahedron 4	$\begin{bmatrix} t_1 \\ t_2 \\ t_3 \end{bmatrix} = \begin{bmatrix} \frac{\sqrt{6}}{2} & -\frac{\sqrt{2}}{2} & 0 \\ -\frac{\sqrt{6}}{2} & -\frac{\sqrt{2}}{2} & 0 \\ \frac{\sqrt{6}}{6} & \frac{\sqrt{2}}{2} & -\sqrt{3} \end{bmatrix} \begin{bmatrix} v_\alpha^* T_s \\ v_\beta^* T_s \\ v_o^* T_s \end{bmatrix} \times \frac{1}{v_{dc}}$ $T_4 = T_s - T_1 - T_2 - T_3$	$v_\gamma \le \frac{v_a}{\sqrt{2}} + \sqrt{\frac{3}{2}} v_\beta$ $v_\gamma > \frac{v_a}{\sqrt{2}} - \sqrt{\frac{3}{2}} v_\beta - \sqrt{3} v_{dc}$

Prism 6	On duration time inter vals	Condition of localisation
Tetrahedron 1	$\begin{bmatrix} t_1 \\ t_2 \\ t_3 \end{bmatrix} = \begin{bmatrix} -\frac{\sqrt{6}}{6} & \frac{\sqrt{6}}{6} & \frac{\sqrt{3}}{3} \\ 0 & -\frac{\sqrt{2}}{2} & 0 \\ \frac{\sqrt{6}}{2} & \frac{\sqrt{2}}{2} & 0 \end{bmatrix} \begin{bmatrix} v_\alpha^* T_s \\ v_\beta^* T_s \\ v_o^* T_s \end{bmatrix} \times \frac{1}{v_{dc}}$ $T_4 = T_s - T_1 - T_2 - T_3$	$v_\gamma \le -\sqrt{2} v_\alpha + \sqrt{3} v_{dc}$ $v_\gamma > \frac{v_a}{\sqrt{2}} - \sqrt{\frac{3}{2}} v_\beta$
Tetrahedron 2	$\begin{bmatrix} t_1 \\ t_2 \\ t_3 \end{bmatrix} = \begin{bmatrix} -\frac{\sqrt{6}}{6} & -\frac{\sqrt{2}}{2} & \frac{\sqrt{3}}{3} \\ -\frac{\sqrt{6}}{2} & -\frac{\sqrt{2}}{2} & 0 \\ -\frac{\sqrt{6}}{6} & -\frac{\sqrt{2}}{2} & -\frac{\sqrt{3}}{3} \end{bmatrix} \begin{bmatrix} v_\alpha^* T_s \\ v_\beta^* T_s \\ v_o^* T_s \end{bmatrix} \times \frac{1}{v_{dc}}$ $T_4 = T_s - T_1 - T_2 - T_3$	$v_\gamma \le \frac{v_a}{\sqrt{2}} - \sqrt{\frac{3}{2}} v_\beta$ $v_\gamma > \frac{v_a}{\sqrt{2}} + \sqrt{\frac{3}{2}} v_\beta$
Tetrahedron 3	$\begin{bmatrix} t_1 \\ t_2 \\ t_3 \end{bmatrix} = \begin{bmatrix} \frac{\sqrt{6}}{3} & 0 & -\frac{\sqrt{3}}{3} \\ 0 & -\sqrt{2} & 0 \\ \frac{\sqrt{6}}{6} & \frac{\sqrt{2}}{2} & \frac{\sqrt{3}}{3} \end{bmatrix} \begin{bmatrix} v_\alpha^* T_s \\ v_\beta^* T_s \\ v_o^* T_s \end{bmatrix} \times \frac{1}{v_{dc}}$ $T_4 = T_s - T_1 - T_2 - T_3$	$v_\gamma \le \frac{v_a}{\sqrt{2}} + \sqrt{\frac{3}{2}} v_\beta$ $v_\gamma > -\sqrt{2} v_\alpha$
Tetrahedron 4	$\begin{bmatrix} t_1 \\ t_2 \\ t_3 \end{bmatrix} = \begin{bmatrix} 0 & -\sqrt{2} & 0 \\ \frac{\sqrt{6}}{2} & \frac{\sqrt{2}}{2} & 0 \\ -\frac{\sqrt{6}}{3} & 0 & \frac{\sqrt{3}}{3} \end{bmatrix} \begin{bmatrix} v_\alpha^* T_s \\ v_\beta^* T_s \\ v_o^* T_s \end{bmatrix} \times \frac{1}{v_{dc}}$ $T_4 = T_s - T_1 - T_2 - T_3$	$v_\gamma \le -\sqrt{2} v_\alpha$ $v_\gamma > \frac{v_a}{\sqrt{2}} - \sqrt{\frac{3}{2}} v_\beta - \sqrt{3} v_{dc}$

Abstract

The four-leg inverter presents a best topology for inverters operating in four-wire distribution systems. The objective of this work is to design a controller circuit based on three-dimensional space vector modulation for a three-phase four-leg inverter. The implementation is performed on Zynq 7020 FPGA board using hardware description language (VHDL). XILINX FPGA provides a very attractive highlevel design/simulation tool called as Xilinx ISE; it is a very flexible tool, which allows testing of a highlevel structural description of the design and make possibilities for quick changes and corrections in the design.

Keywords

Four-leg inverter, Four-wire distribution systems, Three-dimensional space vector modulation, FPGA.

ملخص

إن العاكس رباعي الأرجل يمثل أفضل طبولوجيا للمحولات التي تعمل في أنظمة التوزيع ذات أربعة أسلاك. الهدف من هذا العمل هو تصميم دارة تحكم تعتمد على التعديل الشعاعي للنبضة ثلاثية الابعاد من أجل العاكس ذي أربعة أرجل. يتم التنفيذ على لوحة FPGA 7020 Zynqباستخدام لغة وصف الأجهزة .)VHDL(يوفر XILINX FPGAأداة تصميم / محاكاة عالية المستوى جذابة للغاية تسمى ISE Xilinx؛ التي تمثل أداة مرنة للغاية، تسمح باختبار وصف الهيكلية عالية المستوى للتصميم وإتاحة إمكانية للتغييرات السريعة والتصحيحات في التصميم.

كلمات مفتاحية:

عاكس ذي أربعة أرجل، أنظمة التوزيع ذات أربعة أسلاك، التعديل الشعاعي لعرض النبضة ثلاثي الابعاد .FPGA