Democratic and Popular Republic of Algeria

UNIVERSITY OF KASDI MERBAH -OUARGLA

Faculty of new Technologies of Information and Communication
Department of Electronics and Telecommunication

Submitted in Partial Fulfillment of the Requirement

For an Academic Master Degree

DISSERTATION

ACADEMIC MASTER

Domain: Electronics
Specialty: Electronics Embedded systems

Submitted by:

CHELIGHEM Mohamed CHAHED Abd elhakim Yakoub

TITLE

FPGA-Based Design and Implementation of Space Vector Modulation for Three-Phase Three-Level NPC Inverter

Publically defended

On : 26/06/2018

Before the jury:

Mr : MELHEGUEG Nacer	MAA	President	UKM Ouargla
Mr : KADRI Farid	MAA	Examiner	UKM Ouargla
Mr : BOUZIDI Mansour	MCB	Supervisor	UKM Ouargla

Academic Year : 2017/2018

Dedication

We have a great pleasure to dedicate this modest work

To our Beloved Mothers, our Fathers

To our Dear Sisters, Brothers, Uncles, Aunts and Cousins

To all our Friends

To all our Teachers from primary school to our last year of university

And to all with whom we spent wonderful moments

Acknowledgement

We want absolutely to express our thanks and deep gratitude

to our supervisor Dr. BOUZIDI Mansour,

for his consistent support, orientation, advices and encouragement during the accomplishment of this project.

we would like to thank all the people who contributed in any way to the work described in this thesis.

Contents

List of Abbreviations

HVDC	High-Voltage Direct-Current
PWM	Pulse Width Modulation
DC	Direct Current
IGBT	Insulated Gate Bipolar Transistor
AC	Alternating Current
NPC	Naturel Point Clamped
THD	Total Harmonic Distortion
EMI	Electromagnetic Interface
SVPWM	Space Vector Pulse Width Modulation
SVM	Space Vector Modulation
DSP	Digital Signal Processor
FPGA	Field Programmable Gate Array
LE	Logic Element
VHDL	Very-High-speed integrated Hardware Description Language
CLB	Configurable Logic Block
HDL	Hardware Description Language
IOB	Input Output Block
ISE	Integrated Synthesis Environment
RTL	Register-Transfer Level
PS	Processing System
PL	Programmable Logic
CLK	Clock
LUT	Look Up Tables
GND	Ground

List of Symbols

v	Output Voltage Vector
v_{dc}	DC source voltage
α	Real axis
β	Imaginary axis
U_{ab}, U_{bc}, U_{ca}	Line-to-line voltages
v_{a0}, v_{b0}, v_{c0}	Outputs inverter phase voltages
F_{x0}, F_{x1}, F_{x2}	Switching functions
v^*	Reference voltage vector
ω	Angular frequency
V_m	Amplitude
T_s	Switching period
t_i	Duration time
v_β^*, v_α^*	Coordinate of the reference voltage vector
$\Delta_1, \Delta_2, \Delta_3$	Equations of straight lines

List of Figures

List of tables

General introduction

Recently, multilevel topologies caught great attention in the field of high-power and high-voltage applications[1][2]. They improve output waveform quality of the voltage source inverter by increasing waveform steps and reduce the voltage stress across switches. Low voltage stress results in the low *dv*/*dt*, which causes less EMI problems. Researchers conducted intensive studies on this type inverter, covering soft switching and all kinds of modulations [3][4]. As one of most promising modulation technologies in three phase systems, space vector modulation (SVM) for three-level inverter has an advantage over sinusoidal PWM in voltage utility [5]. Although three-level SVM technique is derived from two-level SVM, three-level SVM is considerably more complex than that of two-level inverter because of large number of inverter switches and the problem of neutral point voltage self-balancing [5]. Due to its complexity in computation, the implementation of the three-level SVM algorithm requires capable digital processor techniques.

Nowadays, microcontrollers and digital signal processors (DSP) are playing a dominating part in the applications for power electronics and motion control, due to their advantages, such as software flexibility, mature application, satisfying performance and low cost [6]. However, the microcontrollers even DSPs may not meet the demanding control requirements on the premise of restricting their setup costs and development time to an acceptable range in the field of electrical and electronic product development. The author in [7] carries out a comparative analysis between DSPs and FPGA-based control capacities in PWM power converters and gives the conclusion that FPGA-based digital control is better than DSP ones for all the comparative terms in his practical experiments. The emergence of field programmable

gate array (FPGA), offering an appropriate solution for improving the performance of controllers, is now considered by an increasing number of designers in various fields of application, such as telecommunication, signal processing, active filtering, power electronics and electric drives [x].

The objective of this thesis is to present an FPGA based implementation of space vector modulation for three-level diode clamped inverter. The three-level inverter using SVM control has superior performance though bringing about much computational complexity. Therefore, the XILINX Zynq 7020 FPGA-based implementation could solve this problem well.

In order to achieve the thesis objective, this thesis is divided into three chapters, which are summarized as follows:

The first chapter is devoted to present the operating principle and mathematical modeling of two and three-level diode clamped inverters.

The space vector modulation (SVM) scheme for two and three-level inverters is discussed in detail in chapter two.

The third chapter is reserved to the implementation of the three-level space vector modulation for three-level inverter using FPGA technology.

Finally, a main conclusion and some recommendations for future works are provided.

Chapter I

Modeling and analysis of two and three-phase three-level NPC inverters

I.1. Introduction

Multilevel converters are finding increased attention in industry and academia as one of the preferred choices of electronic power conversion for high-power applications [8]. They have successfully made their way into the industry and therefore can be considered a mature and proven technology. Currently, they are commercialized in standard and customized products that power a wide range of applications, such as,

variable speed motor drives, reactive power compensation, high-voltage direct-current (HVDC) transmission, wind energy conversion, and railway traction . . . etc. [9].

A multilevel converter has several advantages over a conventional two-level converter that uses high switching frequency pulse width modulation (PWM) such as:

- Lower common mode voltage;
- Lower voltage stress on power switches;
- Lower harmonic contents in output voltage and current.

Unfortunately, multilevel converters have some disadvantages. One particular disadvantage is the greater number of power semiconductor switches needed. Although lower voltage rated switches can be utilized in a multilevel converter, each switch requires a related gate drive circuit. This may cause the overall system to be more expensive and complex.

There are three basic multilevel converter topologies: diode clamped, flying capacitor, and cascaded H-bridge with separate DC sources. Among these topologies, diode-clamped converters are especially interesting because of their simplicity; the multiple voltage levels are generated passively through a set of series-connected capacitors. The simplest family member, the three-level converter, has been widely studied [10].

This chapter presents the operating principle and mathematical modeling of two and three-level diode clamped inverters.

I.2. Two-level inverter

I.2.1. Power circuit of two-level inverter

The power circuit diagram for a two-level inverter is shown in figure (I.1). The inverter is composed of six IGBT transistors with a freewheeling diode in parallel with each active switch to ensure bidirectional flow of the output current. Each leg of the three-phase inverter has upper and lower switches. The lower switches of the three legs are complementary to the upper switches in order to avoid short-circuiting the DC source.

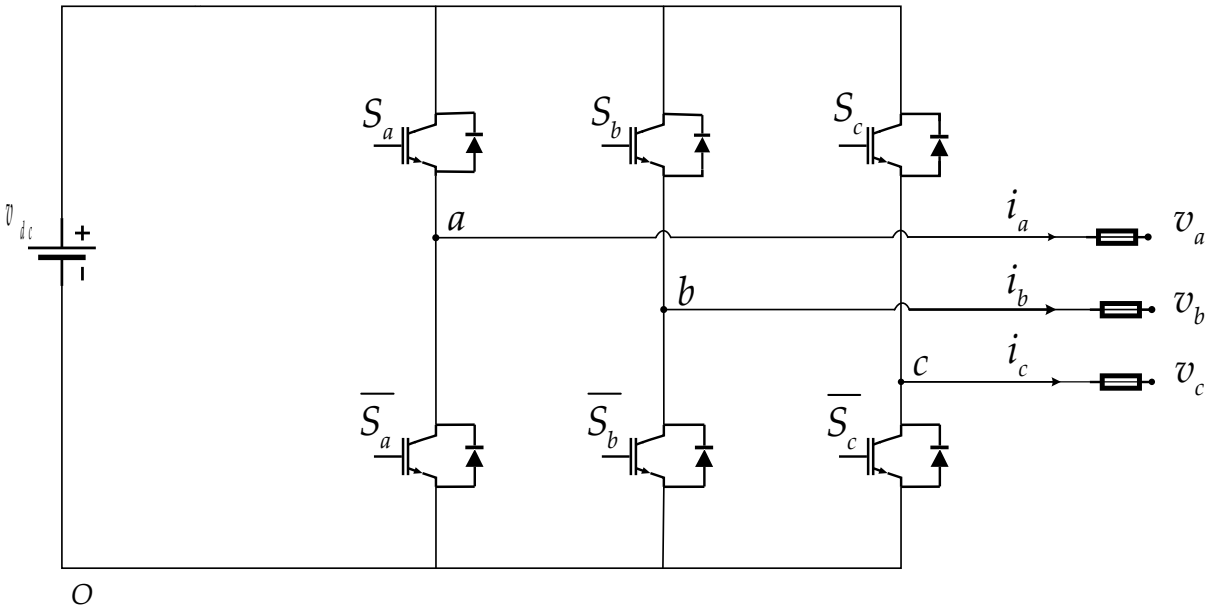


Figure (I.1): Power circuit of three-phase two-level inverter

I.2.2. Output voltages of two-level inverter

Table (I.1) shows that each leg of the three-phase inverter has two switching states, if the upper switch is turned ON (S_x=1, *x=a, b* or *c*) then the voltage $v_{xo} = v_{dc}$, and if this switch is turned OFF (S_x=0) the voltage $v_{xo} = 0$.

Table (I.1): Switching states of one leg of two-level inverter (*x =a, b or c*)

Switching states	S_x	**Output Phase voltage** v_{xo}
1	*1*	v_{dc}
0	*0*	0

The phase to phase output voltages of two-level inverter can be described with the help of figure (I.1):

$$\begin{aligned} U_{ab} &= (S_a - S_b)v_{dc} \\ U_{bc} &= (S_b - S_c)v_{dc} \\ U_{ca} &= (S_c - S_a)v_{dc} \end{aligned} \quad \text{(I.1)}$$

The output voltages can be obtained by:

$$\begin{bmatrix} v_a \\ v_b \\ v_c \end{bmatrix} = \frac{1}{3}\begin{bmatrix} U_{ab} - U_{ca} \\ U_{bc} - U_{ab} \\ U_{ca} - U_{bc} \end{bmatrix} \tag{I.2}$$

Using equation (I.1), (I.2) can be written as:

$$\begin{bmatrix} v_a \\ v_b \\ v_c \end{bmatrix} = \frac{v_{dc}}{3}\begin{bmatrix} 2 & -1 & -1 \\ -1 & 2 & -1 \\ -1 & -1 & 2 \end{bmatrix}\begin{bmatrix} S_a \\ S_b \\ S_c \end{bmatrix} \tag{I.3}$$

I.2.3. Output voltage vector and space vector representation

The complex form of the output voltage is given by:

$$v = v_a e^{j0} + v_b e^{-j2\pi/3} + v_c e^{-j4\pi/3} \tag{I.4}$$

After transforming the three-phase system in a two-phase system by the *Concordia* transformation, we can represent the vector v in a two-dimensional space (α, β) by:

$$v = v_\alpha + jv_\beta \tag{I.5}$$

Where v_α and v_β are the projections of the vector v in the (α, β) space given by:

$$\begin{bmatrix} v_\alpha \\ v_\beta \end{bmatrix} = \sqrt{\frac{2}{3}}\begin{bmatrix} 1 & -1/2 & -1/2 \\ 0 & \sqrt{3}/2 & -\sqrt{3}/2 \end{bmatrix}\begin{bmatrix} v_a \\ v_b \\ v_c \end{bmatrix} \tag{I.6}$$

Table (I.1) shows the different switching states of the inverter and the coordinates of the output voltage vector v_i corresponding to each state.

Table (I.2): Switching states of the two-level inverter and the coordinates of the output voltage vector v_i

S_a	S_b	S_c	v_α	v_β	v_i
0	0	0	0	0	v_0
1	0	0	$\sqrt{2/3}v_{dc}$	0	v_1
1	1	0	$\sqrt{1/6}v_{dc}$	$\sqrt{1/2}v_{dc}$	v_2
0	1	0	$-\sqrt{1/6}v_{dc}$	$\sqrt{1/2}v_{dc}$	v_3
0	1	1	$-\sqrt{2/3}v_{dc}$	0	v_4
0	0	1	$-\sqrt{1/6}v_{dc}$	$-\sqrt{1/2}v_{dc}$	v_5
1	0	1	$-\sqrt{1/6}v_{dc}$	$-\sqrt{1/2}v_{dc}$	v_6
1	1	1	$\sqrt{1/6}v_{dc}$	0	v_7

As shown in table (I.2), there are six active vectors v_1 to v_6 (the combination of the inverter's switches leads to a non-zero output voltage), whereas the other two vectors are null vectors v_0 and v_7 (all phases are connected to the same point). The graphical representation is shown in figure (I.2).

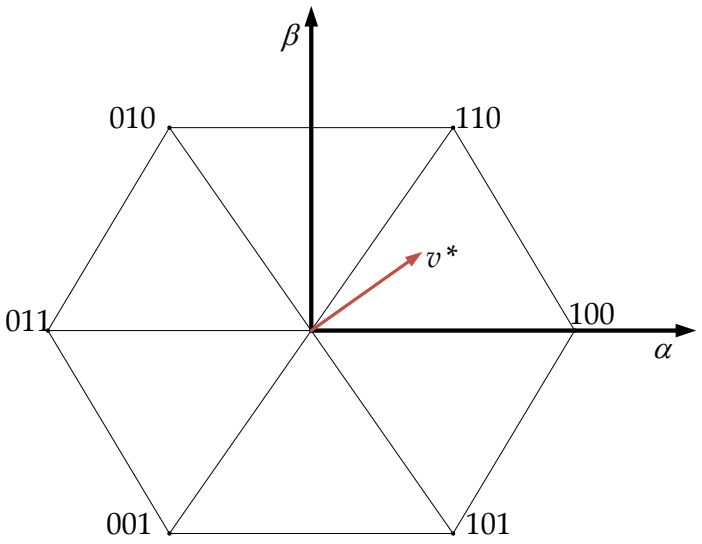


Figure (I.2): Space vector representation of different switching voltage vectors available at the inverter's AC-side in a two-level inverter

I.3. Three-level diode clamped inverter

The three-level NPC inverter features higher operating voltage without devices in series, better output voltage THD, and lower electromagnetic interference (EMI). Therefore, it is increasingly used in high power applications. In this section, the power circuit and the switching states of this type of inverter are introduced.

I.3.1. Power circuit of three-level inverter

The power circuit of three-level inverter is shown in figure (I.3). There are four switching devices (S_{x1}, S_{x2}, S_{x3} and S_{x4}), four anti-parallel diodes (D_{x1}, D_{x2}, D_{x3} and D_{x4}) and two clamping diodes (D_{x5} and D_{x6}) in each leg, where the index x represents legs a, b or c, respectively. On the DC side of the inverter, the DC bus is composed of two identical voltage sources providing a neutral point o.

In order to avoid short-circuiting the DC source of the three-level inverter, there are two complimentary switch pairs for each leg $\left(S_{x3}, \overline{S}_{x1}\right)$, $\left(S_{x4} = \overline{S}_{x2}\right)$.

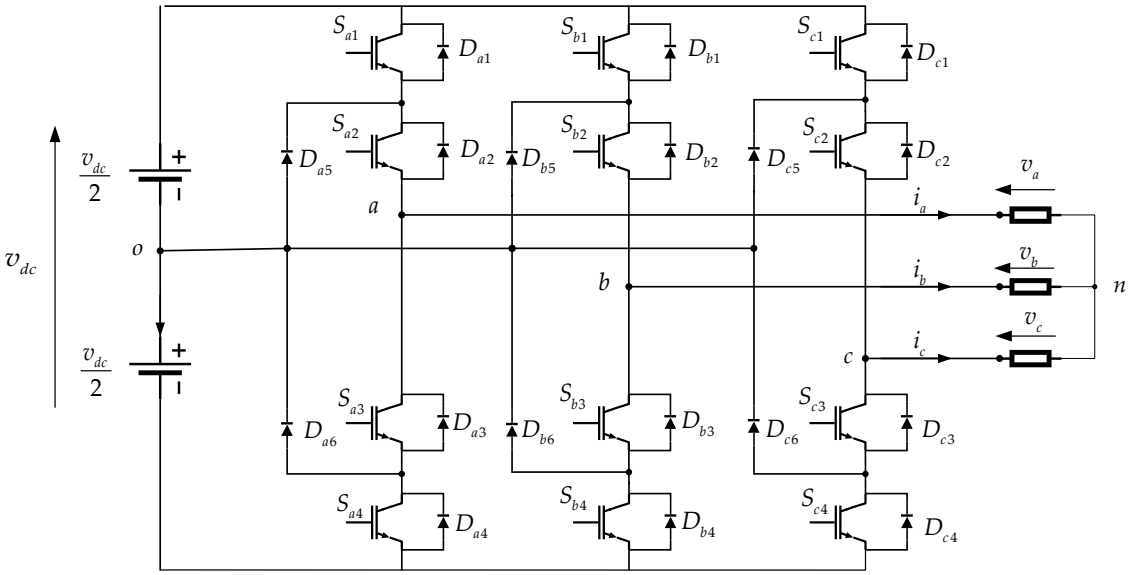


Figure (I.3): Power circuit of three-level diode clamped inverter

I.3.2. Output voltages of three-level inverter

In three-level inverters, the phase voltage is defined as the voltage between the phase output and the neutral point o, and is determined by three per-phase switching states, "2", "1" and "0", which are shown in figure (I.4).

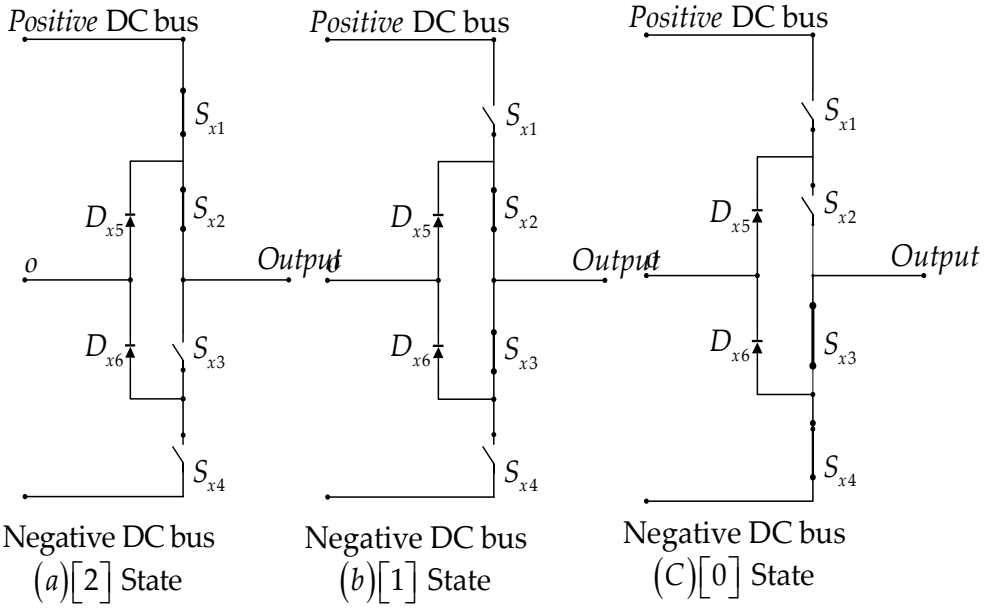


Figure (I.4): Three switching states of each phase

The switching combinations of each leg are summarized in table (I.3).

Table (I.3): Switching states of one leg of three-level inverter (*x =a, b or c*)

Switching states	S_{x1}	S_{x2}	S_{x3}	S_{x4}	**Output Phase voltage** v_{xo}
2	*1*	*1*	*0*	*0*	$v_{dc}/2$
1	*0*	*1*	*1*	*0*	0
0	*0*	*0*	*1*	*1*	$-v_{dc}/2$

In three-level inverter, each leg has three switching functions, which be expressed as:

$$\begin{aligned} F_{x2} &= S_{x2}S_{x1} \\ F_{x1} &= S_{x2}\overline{S}_{x1} \\ F_{x0} &= \overline{S}_{x2}\overline{S}_{x1} \end{aligned} \tag{I.7}$$

The instantaneous output inverter phase to middle pointe o v_{ao}, v_{bo} and v_{co} can be expressed as:

$$\begin{bmatrix} v_{ao} \\ v_{bo} \\ v_{co} \end{bmatrix} = \begin{bmatrix} F_{a2} & F_{a1} & F_{a0} \\ F_{b2} & F_{b1} & F_{b0} \\ F_{c2} & F_{c1} & F_{c0} \end{bmatrix} \begin{bmatrix} \frac{v_{dc}}{2} \\ 0 \\ -\frac{v_{dc}}{2} \end{bmatrix} \tag{I.8}$$

The line-to-line voltages, U_{ab}, U_{bc} and U_{ca}, can be obtained through the inverter phase voltages as follows:

$$\begin{bmatrix} U_{ab} \\ U_{bc} \\ U_{ca} \end{bmatrix} = \begin{bmatrix} v_{ao} - v_{bo} \\ v_{bo} - v_{co} \\ v_{co} - v_{ao} \end{bmatrix} \tag{I.9}$$

The voltage between the three-phase balanced load can be obtained by:

$$\begin{bmatrix} v_a \\ v_b \\ v_c \end{bmatrix} = \frac{1}{3} \begin{bmatrix} U_{ab} - U_{ca} \\ U_{bc} - U_{ab} \\ U_{ca} - U_{bc} \end{bmatrix} \tag{I.10}$$

Table (I.4): Three-phase switching states of three-level inverter

Group No	Switching states [abc]	Inverter phase voltage			Line-to-line voltages			Load phase voltages		
		v_{a0}	v_{b0}	v_{c0}	U_{ab}	U_{bc}	U_{ca}	v_{an}	v_{bn}	v_{cn}
0	[000]	$-v_{dc}/2$	$-v_{dc}/2$	$-v_{dc}/2$	0	0	0	0	0	0
	[111]	0	0	0						
	[222]	$v_{dc}/2$	$v_{dc}/2$	$v_{dc}/2$						
1	[211]	$v_{dc}/2$	0	0	0	$v_{dc}/2$	$-v_{dc}/2$	$v_{dc}/3$	$-v_{dc}/6$	$-v_{dc}/6$
	[100]	0	$-v_{dc}/2$	$-v_{dc}/2$						
2	[210]	$v_{dc}/2$	$v_{dc}/2$	0	0	$v_{dc}/2$	$-v_{dc}/2$	$v_{dc}/6$	$v_{dc}/6$	$-v_{dc}/3$
	[110]	0	0	$-v_{dc}/2$						
3	[121]	0	$v_{dc}/2$	0	$-v_{dc}/2$	$v_{dc}/2$	0	$v_{dc}/6$	$-v_{dc}/3$	$v_{dc}/6$
	[010]	$-v_{dc}/2$	0	$-v_{dc}/2$						
4	[022]	0	$v_{dc}/2$	$v_{dc}/2$	$-v_{dc}/2$	0	$v_{dc}/2$	$-v_{dc}/3$	$v_{dc}/6$	$v_{dc}/6$
	[122]	$-v_{dc}/2$	0	0						
5	[112]	0	0	$v_{dc}/2$	0	$-v_{dc}/2$	$v_{dc}/2$	$-v_{dc}/6$	$-v_{dc}/6$	$v_{dc}/3$
	[001]	$-v_{dc}/2$	$-v_{dc}/2$	0						
6	[212]	$v_{dc}/2$	0	$v_{dc}/2$	$v_{dc}/2$	$-v_{dc}/2$	0	$v_{dc}/6$	$-v_{dc}/3$	$v_{dc}/6$
	[101]	0	$-v_{dc}/2$	0						
7	[210]	$v_{dc}/2$	0	$-v_{dc}/2$	$v_{dc}/2$	$v_{dc}/2$	v_{dc}	$v_{dc}/2$	0	$-v_{dc}/2$
8	[120]	0	$v_{dc}/2$	$-v_{dc}/2$	$-v_{dc}/2$	v_{dc}	$-v_{dc}/2$	0	$v_{dc}/2$	$-v_{dc}/2$
9	[021]	$-v_{dc}/2$	$v_{dc}/2$	0	$-v_{dc}$	$v_{dc}/2$	$v_{dc}/2$	$-v_{dc}/2$	$v_{dc}/2$	0
10	[012]	$-v_{dc}/2$	0	$v_{dc}/2$	$-v_{dc}/2$	$-v_{dc}/2$	v_{dc}	$-v_{dc}/2$	0	$v_{dc}/2$
11	[102]	0	$-v_{dc}/2$	$v_{dc}/2$	$v_{dc}/2$	$-v_{dc}$	$v_{dc}/2$	0	$-v_{dc}/2$	$v_{dc}/2$
12	[201]	$v_{dc}/2$	$-v_{dc}/2$	0	v_{dc}	$-v_{dc}/2$	$-v_{dc}/2$	$v_{dc}/2$	$-v_{dc}/2$	0
13	[200]	$v_{dc}/2$	$-v_{dc}/2$	$-v_{dc}/2$	v_{dc}	0	$-v_{dc}/2$	$2v_{dc}/3$	$-v_{dc}/3$	$-v_{dc}/3$
14	[220]	$v_{dc}/2$	$v_{dc}/2$	$-v_{dc}/2$	0	v_{dc}	$-v_{dc}$	$v_{dc}/3$	$v_{dc}/3$	$-2v_{dc}/3$
15	[020]	$-v_{dc}/2$	$v_{dc}/2$	$-v_{dc}/2$	$-v_{dc}$	v_{dc}	0	$-v_{dc}/3$	$2v_{dc}/3$	$-v_{dc}/3$
16	[022]	$-v_{dc}/2$	$v_{dc}/2$	$v_{dc}/2$	$-v_{dc}$	0	v_{dc}	$-2v_{dc}/3$	$v_{dc}/3$	$v_{dc}/3$
17	[002]	$-v_{dc}/2$	$-v_{dc}/2$	$v_{dc}/2$	0	$-v_{dc}$	v_{dc}	$-v_{dc}/3$	$-v_{dc}/3$	$2v_{dc}/3$
18	[202]	$v_{dc}/2$	$-v_{dc}/2$	$v_{dc}/2$	v_{dc}	$-v_{dc}$	0	$v_{dc}/3$	$-2v_{dc}/$	$v_{dc}/3$

According to the line-to-line voltages and the load phase voltages, the inverter switching states are classified into 19 groups as shown in table (I.4), in which some groups have two or three inverter switching states although their inverter phase voltages are different, these states are called redundant states.

Particularly, group 0 has three inverter switching states, and each of group 1 to group 6 contains two switching states.

I.3.3. Space vectors of three-level inverter

The coordinates of each switching vector, v_α, v_β are calculated using the matrix transformation (I.6). Table (I.5) shows the different switching states of the three-level inverter and the coordinates of the output voltage vector v_i corresponding to each switching state.

Table (I.5): Space vectors and corresponding switching states in $\alpha\beta$ plane

Switching states	$v_{\alpha i}$	$v_{\beta i}$	v_i
222,111,000	0	0	v_0^a, v_0^b, v_0^c
211,100	$\sqrt{1/6}v_{dc}$	0	v_1^a, v_1^b
200	$\sqrt{2/3}v_{dc}$	0	v_2
210	$\sqrt{3/8}v_{dc}$	$\sqrt{1/8}v_{dc}$	v_3
221,110	$\sqrt{1/24}v_{dc}$	$\sqrt{1/8}v_{dc}$	v_4^a, v_4^b
220	$\sqrt{1/6}v_{dc}$	$\sqrt{1/2}v_{dc}$	v_5
120	0	$\sqrt{1/2}v_{dc}$	v_6
121,010	$-\sqrt{1/24}v_{dc}$	$\sqrt{1/8}v_{dc}$	v_7^a, v_7^b
020	$-\sqrt{1/6}v_{dc}$	$\sqrt{1/2}v_{dc}$	v_8
021	$-\sqrt{3/8}v_{dc}$	$\sqrt{1/8}v_{dc}$	v_9
122,011	$-\sqrt{1/6}v_{dc}$	0	v_{10}^a, v_{10}^b
022	$-\sqrt{2/3}v_{dc}$	0	v_{11}
012	$-\sqrt{3/8}v_{dc}$	$-\sqrt{1/8}v_{dc}$	v_{12}
112,001	$-\sqrt{1/24}v_{dc}$	$-\sqrt{1/8}v_{dc}$	v_{13}^a, v_{13}^b
002	$-\sqrt{1/6}v_{dc}$	$-\sqrt{1/2}v_{dc}$	v_{14}
102	0	$-\sqrt{1/2}v_{dc}$	v_{15}

All 27 switching states represented in table (I.5) can be described using a graphical representation in two-dimensional space α-β as shown in figure (I.5).

Based on their magnitudes, the 19 space vectors correspond to the 27 switching states of the three-level inverter, which can be further classified into four types, zero vector, small vectors, medium vectors, and large vectors.

The diagram of space vectors of figure (I.5) can be divided into six sectors, and each sector is divided into four triangle.

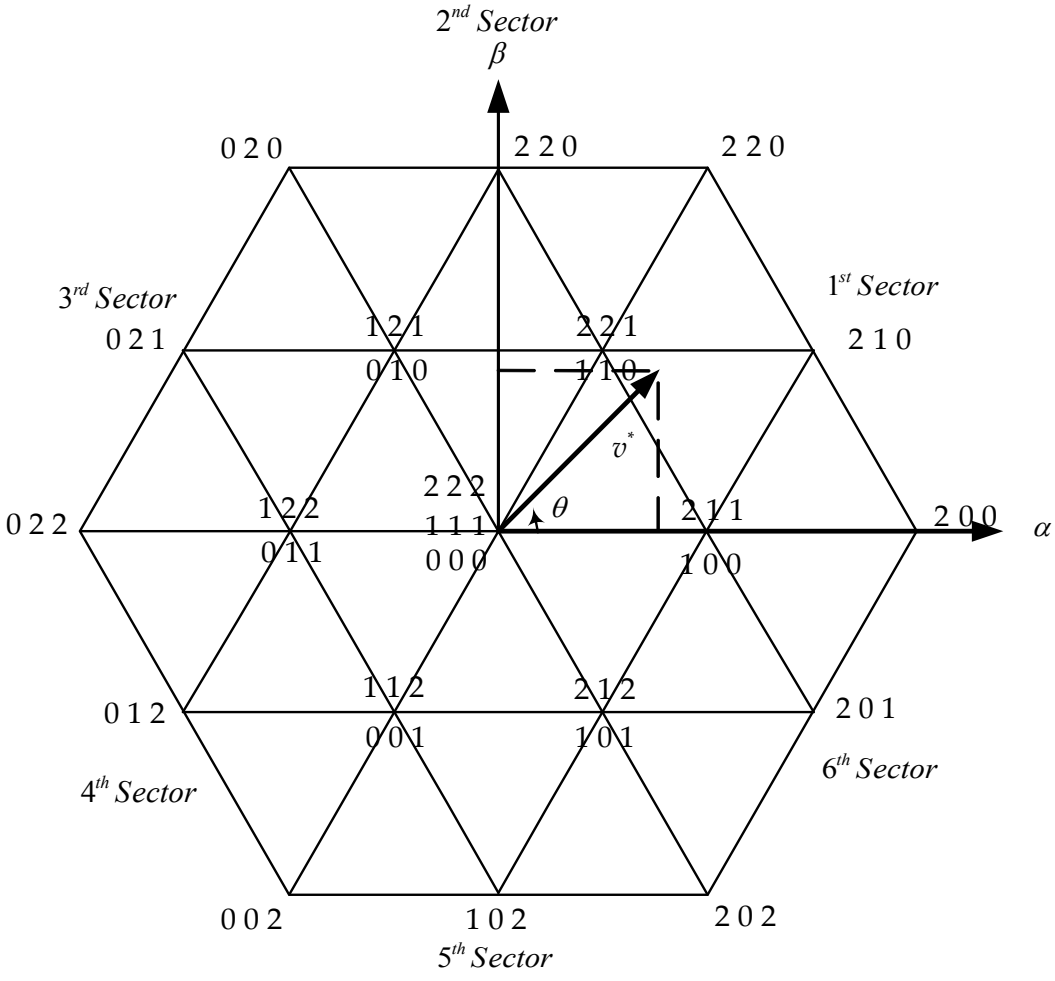


Figure (I.5): Space voltage vectors for a three-level inverter

I.4. Conclusion

In this chapter a comprehensive analysis of the two and three-level inverter, including the inverter configurations, basic principles, and mathematical modeling have been provided.

The next chapter will be devoted to the application of space vector modulation to control the two and three level inverter.

Chapter II

Space vector modulation of three-phase three-level NPC inverter

II.1. Introduction

The output voltage waveforms in multilevel inverters can be generated at low switching frequencies with high efficiency and low distortion. In recent years, beside multilevel inverters various pulse width modulation (PWM) techniques have been also developed [11]. Carrier based PWM, hysteresis current control, and selective harmonic elimination [11]. Among these PWM techniques, space vector modulation technique is one of the most popular techniques gained interest recently. Compared with the above mentioned PWM techniques, the space vector modulation in general provides the following features:

- Low harmonics distortion of output voltage and current;
- Better utilization of the DC bus voltage;
- Easy digital implementation.

In this chapter, the space vector modulation scheme for two and three-level inverter is discussed in detail.

II.2. Space vector modulation for two level inverter

A SVM is a discrete type of modulation technique in which a sampled reference vector, v^*, is synthesized by the time average of a number of appropriate switching vectors. The space vector modulation has three main steps:

1- Reference voltage vector location;
2- Duration time calculation;
3- Pulses creation.

II.2.1. Reference voltage vector

The reference voltages are generally three phase balance voltages given by the following system:

$$\begin{aligned} v_a^* &= V_m \sin \omega t \\ v_b^* &= V_m \sin\left(\omega t - \frac{2\pi}{3}\right) \\ v_c^* &= V_m \sin\left(\omega t - \frac{4\pi}{3}\right) \end{aligned} \tag{II.1}$$

Where: $\omega = 2\pi f$ is the angular frequency.

The three-phase reference voltages in v_a^*, v_b^*, v_c^* frame can be transformed into a two-dimensional $\alpha\beta$ complex frame by the following transformation:

$$\begin{bmatrix} v_\alpha^* \\ v_\beta^* \end{bmatrix} = \sqrt{\frac{2}{3}} \begin{bmatrix} 1 & -1/2 & -1/2 \\ 0 & \frac{\sqrt{3}}{2} & -\frac{\sqrt{3}}{2} \end{bmatrix} \begin{bmatrix} v_a^* \\ v_b^* \\ v_c^* \end{bmatrix} \tag{II.2}$$

Projection of three-phase reference voltages into the $\alpha\beta$ plane is a vector called the reference voltage vector $v^* = \begin{bmatrix} v_\alpha^* & v_\beta^* \end{bmatrix}^T$, it rotates counterclockwise in space diagram with angular frequency of ω as shown in figure (II.1).

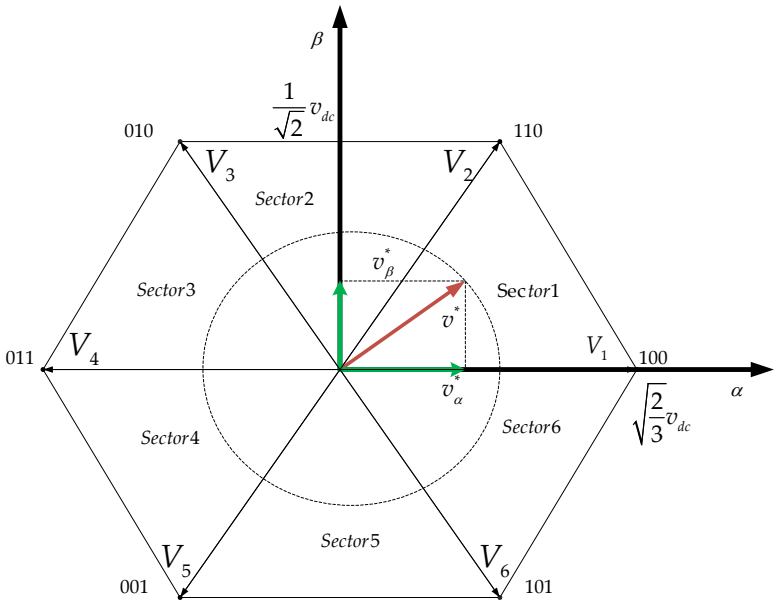


Figure (II.1): Two-level inverter space vector diagram and reference voltage vector trajectory

II.2.2. Reference voltage vector location

As shown in figure (II.1), the space vector diagram is divided into six sectors; therefore, we must determine the sector number according to the location of the reference voltage.

From the coordinates v_α^*, v_β^*, and using the equations of its two sides (for each sector), we can deduce in which sector the reference voltage vector v^* is located.

Figure (II.2) shows the diagram illustrating the steps of this method.

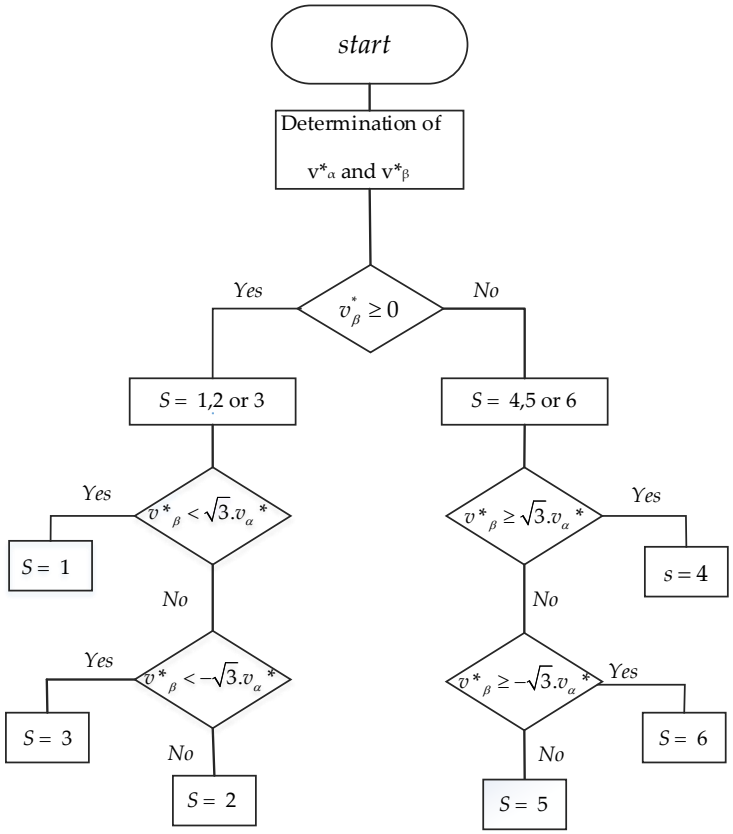


Figure (II.2): Diagram of the sector number identification

II.2.3. Duration time calculation

In order to minimize the switching losses and to reduce the current ripple, switching vectors adjacent to the reference vector should be selected [12]. At any sampling instant, the tip of the voltage vector lies in a sector formed by the three switching vectors. The on-duration time intervals of each vector are obtained in accordance to the average value principle, which is given by [13]:

$$\begin{aligned} v_i t_i + v_{i+1} t_{i+1} + v_0 t_0 &= v^* T_s \\ t_i + t_{i+1} + t_0 &= T_s \end{aligned} \qquad \text{(II.3)}$$

Where T_s is the switching period, v_i, v_{i+1} the two switching vectors adjacent to the reference voltage vector of the sector S_i, v_0 is the zero-switching vector and t_i, t_{i+1}, and t_0 are their on-duration time intervals respectively.

Expression (II.4) can by decomposed in the $\alpha\beta$ coordinates system as follows:

$$\begin{bmatrix} v_{\alpha i} & v_{\alpha i+1} \\ v_{\beta i} & v_{\beta i+1} \end{bmatrix} \begin{bmatrix} t_i \\ t_{i+1} \end{bmatrix} = \begin{bmatrix} v_\alpha^* T_s \\ v_\beta^* T_s \end{bmatrix} \tag{II.4}$$

The duration time of the zero switching vectors (v_0 and v_7) can be deduced as follow:

$$t_0 = T_s - t_i - t_{i+1} \tag{II.5}$$

To simplify the analysis, we define the following three variables *e*, *l* and *k*:

$$\begin{aligned} e &= T_s \frac{\sqrt{3} v_\alpha^* + v_\beta^*}{\sqrt{2} v_{dc}} \\ l &= T_s \frac{\sqrt{3} v_\alpha^* - v_\beta^*}{\sqrt{2} v_{dc}} \\ k &= T_s \frac{\sqrt{2} v_\beta^*}{v_{dc}} \end{aligned} \tag{II.6}$$

The times t_i and t_{i+1} for each sector are expressed as a function of the variables *e*, *l* and *k* according to the table (II.1):

Table (II.1): Switching times of all sectors

Sector S_i	***1***	***2***	***3***	***4***	***5***	***6***
t_i	*e*	*l*	*k*	*-e*	*-l*	*-k*
t_{i+1}	*k*	*-e*	*-l*	*-k*	*e*	*l*

II.2.4. Pulses generation

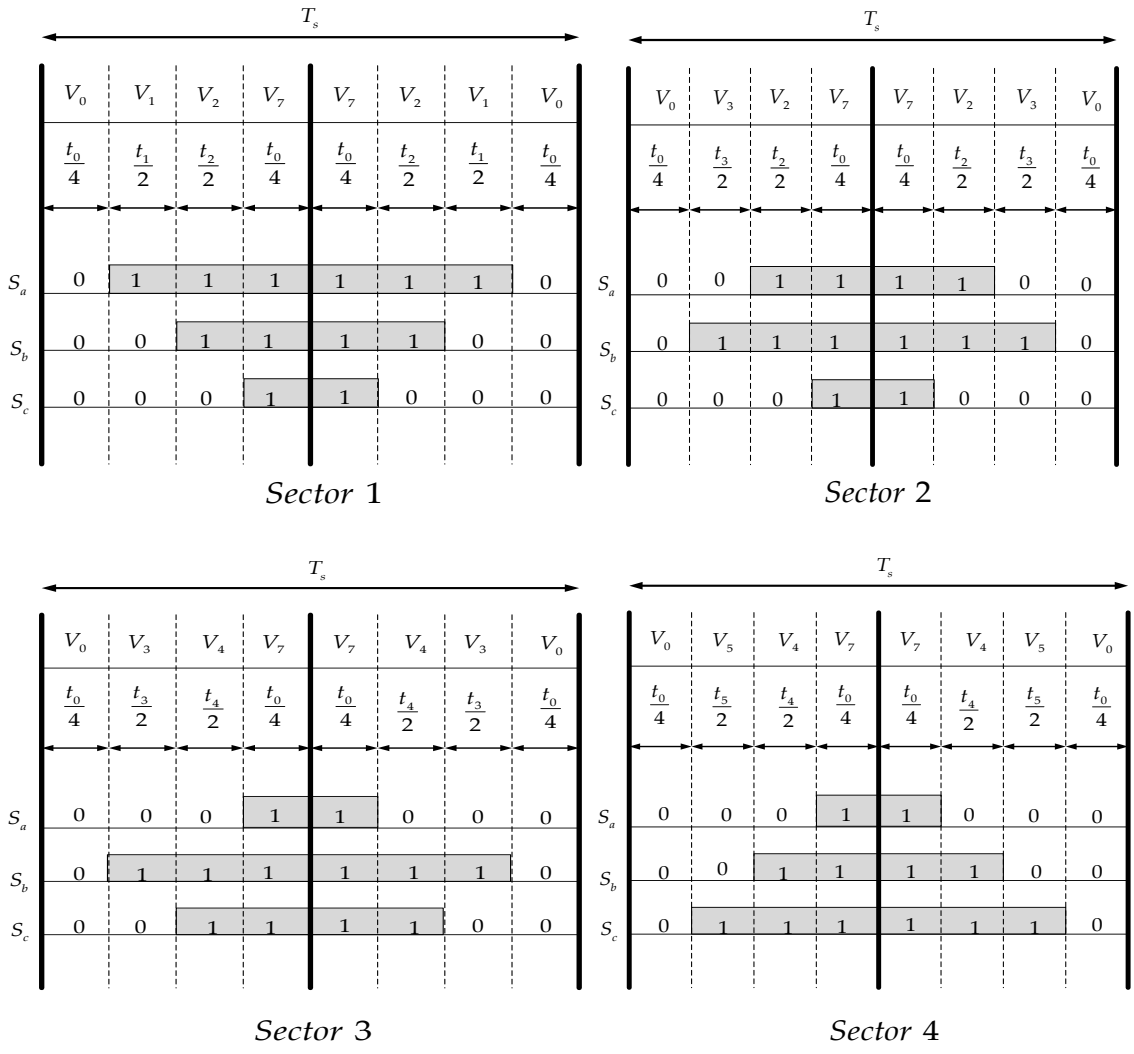
With the proper space vector selected and their duration time calculated, the switching state sequence of the space vector modulation for two-level inverter needs to be

designed in order to achieve the minimum device switching frequency. The adopted symmetrical switching sequence is widely used [14].

The switching period is divided into eight segments to split the applying time of each switching vector evenly.

The switching period always starts by applying the zero switching vector (000), the next applied switching vector is selected so that only one switch state is changed at a time, after the first and the second active switching vectors are applied, the other zero switching vector (111) is followed. After these steps, the sequence is repeated in a reverse order.

Figure (II.3) shows the pulses generation of all sectors.



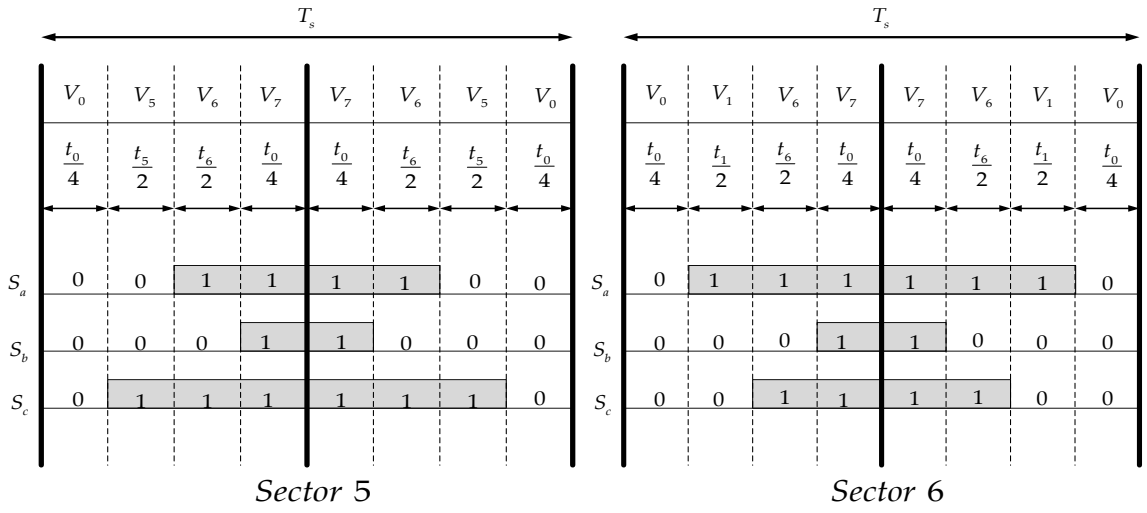


Figure (II.3): Pulses generation in all sectors of two level inverter

II.3. Space vector modulation for three-level inverter

II.3.1. Determination of the space vector location

In three-level space vector modulation, the space vector location is determined in two steps. The first step determines the sector number of where the vector lies. The second step determines the triangle in which the vector lies [12].

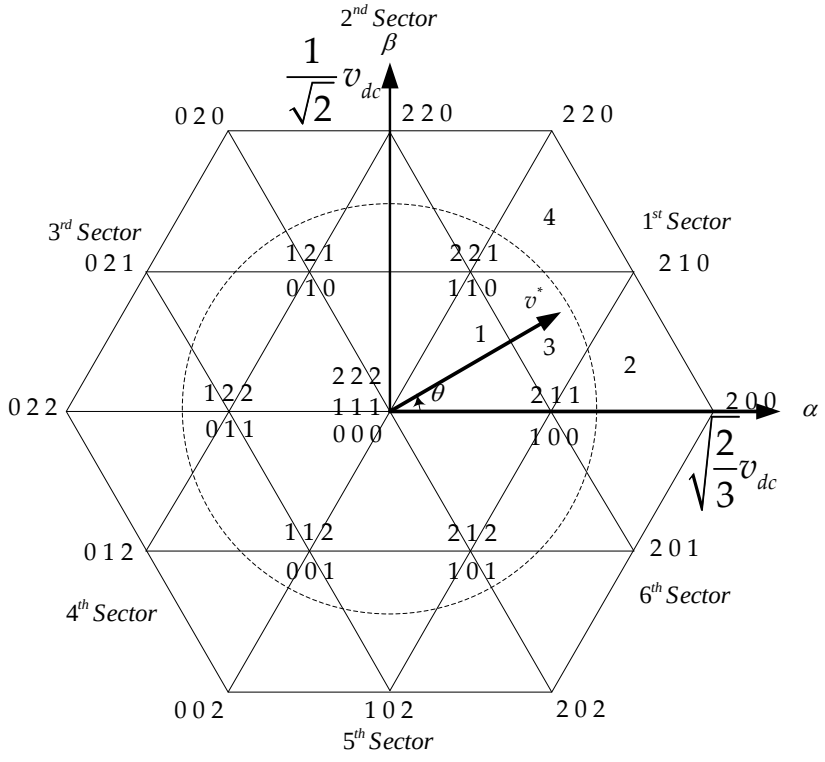


Figure (II.4): Space voltage vectors for a three-level inverter

The sector number can be deduced in the same way as for the two-level inverter. The triangle within each sector is deduced using the equations of its three sides. As shown in figure (II.4), for triangle 1, two sides are already bounded by both sides of the sector. For both triangles 3 and 4 one of the three sides is bounded by one of the two sides of the sector and the other by the outer limit of the hexagon. The third side of the three triangles 1, 2, and 4 is determined as shown in table (II.2). For each sector, if we determine the three triangles 1, 2 and 4, the part of the remaining sector represents triangle 3.

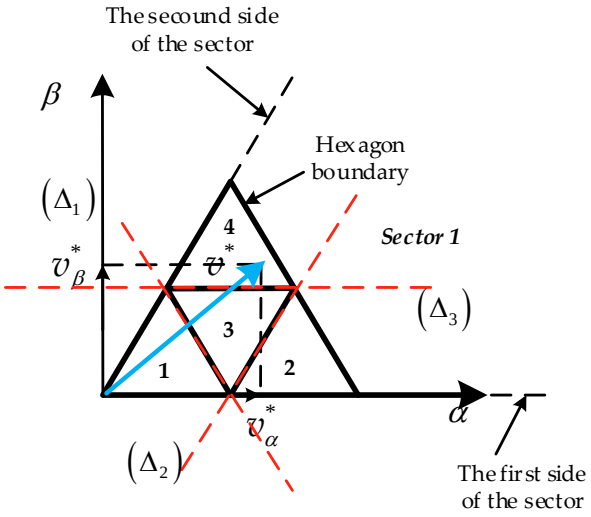


Figure (II.5): Triangles of the first sector

The lines $(\Delta_1),(\Delta_2)$ and (Δ_3) have equations:

$$\begin{aligned}(\Delta_1): v_\beta^* &= -\sqrt{3}v_\alpha^* + \frac{1}{\sqrt{2}}v_{dc} \\ (\Delta_2): v_\beta^* &= \sqrt{3}v_\alpha^* - \frac{1}{\sqrt{2}}v_{dc} \\ (\Delta_3): v_\beta^* &= \frac{1}{2\sqrt{2}}v_{dc}\end{aligned} \qquad \text{(II.7)}$$

Table (II.2): Triangle identification of all sectors

	Triangle 1	*Triangle* 2	*Triangle* 4
Sector 1	$v_\beta^* < -\sqrt{3}v_\alpha^* + \sqrt{1/2}v_{dc}$	$v_\beta^* < \sqrt{3}v_\alpha^* - \sqrt{1/2}v_{dc}$	$v_\beta^* \geq \sqrt{1/8}v_{dc}$
Sector 2	$v_\beta^* < \sqrt{1/8}v_{dc}$	$v_\beta^* \geq -\sqrt{3}v_\alpha^* + \sqrt{1/2}v_{dc}$	$v_\beta^* \geq \sqrt{3}v_\alpha^* + \sqrt{1/2}v_{dc}$
Sector 3	$v_\beta^* < \sqrt{3}v_\alpha^* + \sqrt{1/2}v_{dc}$	$v_\beta^* \geq \sqrt{1/8}v_{dc}$	$v_\beta^* < -\sqrt{3}v_\alpha^* - \sqrt{1/2}v_{dc}$
Sector 4	$v_\beta^* \geq -\sqrt{3}v_\alpha^* - \sqrt{1/2}v_{dc}$	$v_\beta^* \geq \sqrt{3}v_\alpha^* + \sqrt{1/2}v_{dc}$	$v_\beta^* < -\sqrt{1/8}v_{dc}$
Sector 5	$v_\beta^* \geq -\sqrt{1/8}v_{dc}$	$v_\beta^* < -\sqrt{3}v_\alpha^* - \sqrt{1/2}v_{dc}$	$v_\beta^* < \sqrt{3}v_\alpha^* - \sqrt{1/2}v_{dc}$
Sector 6	$v_\beta^* \geq \sqrt{3}v_\alpha^* - \sqrt{1/2}v_{dc}$	$v_\beta^* < \sqrt{1/8}v_{dc}$	$v_\beta^* \geq -\sqrt{3}v_\alpha^* + \sqrt{1/2}v_{dc}$

II.3.2. Duration time calculation

By using the same strategy that was used in two level SVM, when the reference voltage vector is located in a known triangle, the nearest switching vectors are selected to synthesize the reference voltage vector see (figure (II.6)).

$$\begin{aligned} v_x t_x + v_y t_y + v_z t_z &= v^* T_s \\ t_x + t_y + t_z &= T_s \end{aligned} \tag{II.8}$$

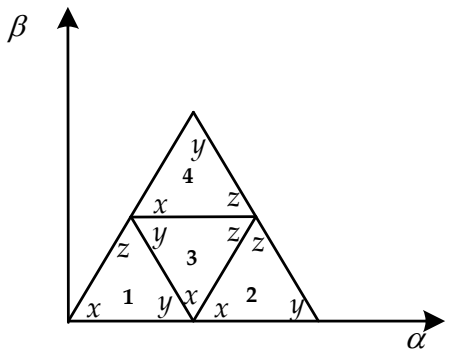


Figure (II.6): Apex *x*, *y* and *z* for each triangle of the first sector

The projection of the vectors v_x, v_y and v^* on the two axes (α, β) gives:

$$\begin{bmatrix} v_{\alpha x} & v_{\alpha y} \\ v_{\beta x} & v_{\beta y} \end{bmatrix} \begin{bmatrix} t_x \\ t_y \end{bmatrix} = \begin{bmatrix} v_\alpha^* T_s \\ v_\beta^* T_s \end{bmatrix} \tag{II.9}$$

And:

$$t_z = T_s - t_x - t_y \tag{II.10}$$

Since the coordinates of the reference voltage vector $\left(v_\alpha^*, v_\beta^*\right)$ are known (Table (I.5)).

It is possible to calculate the duration times, t_x, t_y, and t_z as a function of $\left(v_\alpha^*, v_\beta^*\right)$ and DC voltage v_{dc}. Table (II.3) summarizes the on duration times of all triangles located in the first sector.

The on duration times of all triangles located in all sectors are summarized in table (A.1) of appendix.

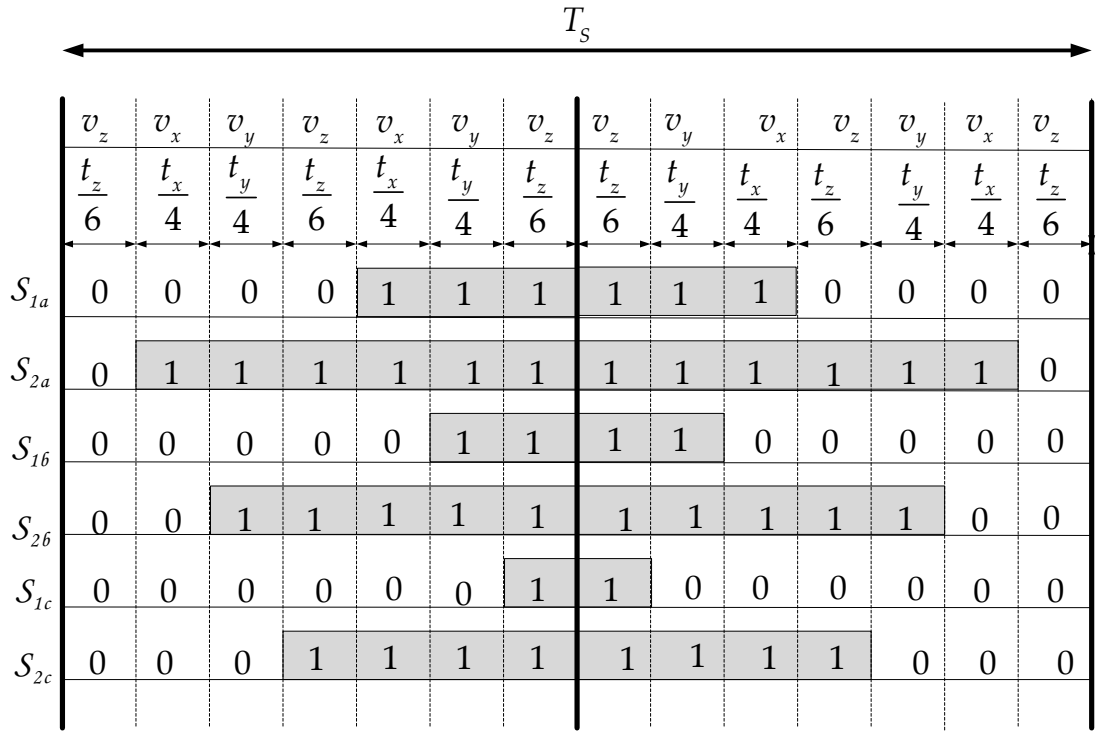
Table (II.3): Duration time intervals of all triangles of the first sector

Triangle 1	$\begin{bmatrix} t_x \\ t_y \end{bmatrix} = \begin{bmatrix} -\sqrt{6} & -\sqrt{2} \\ 0 & 2\sqrt{2} \end{bmatrix} \begin{bmatrix} v_\alpha^* \\ v_\beta^* \end{bmatrix} \frac{T}{v_{dc}}$	***Triangle 2***	$\begin{bmatrix} t_x \\ t_y \end{bmatrix} = \begin{bmatrix} \frac{-\sqrt{6}}{2} & \frac{-3\sqrt{2}}{2} \\ \sqrt{6} & 2\sqrt{2} \end{bmatrix} \begin{bmatrix} v_\alpha^* \\ v_\beta^* \end{bmatrix} \frac{T}{v_{dc}}$
Triangle 3	$\begin{bmatrix} t_x \\ t_y \end{bmatrix} = \begin{bmatrix} 0 & 2\sqrt{2} \\ \sqrt{6} & -\sqrt{2} \end{bmatrix} \begin{bmatrix} v_\alpha^* \\ v_\beta^* \end{bmatrix} \frac{T}{v_{dc}}$	***Triangle 4***	$\begin{bmatrix} t_x \\ t_y \end{bmatrix} = \begin{bmatrix} \sqrt{6} & -\sqrt{2} \\ -\frac{\sqrt{6}}{2} & \frac{-3\sqrt{2}}{2} \end{bmatrix} \begin{bmatrix} v_\alpha^* \\ v_\beta^* \end{bmatrix} \frac{T}{v_{dc}}$

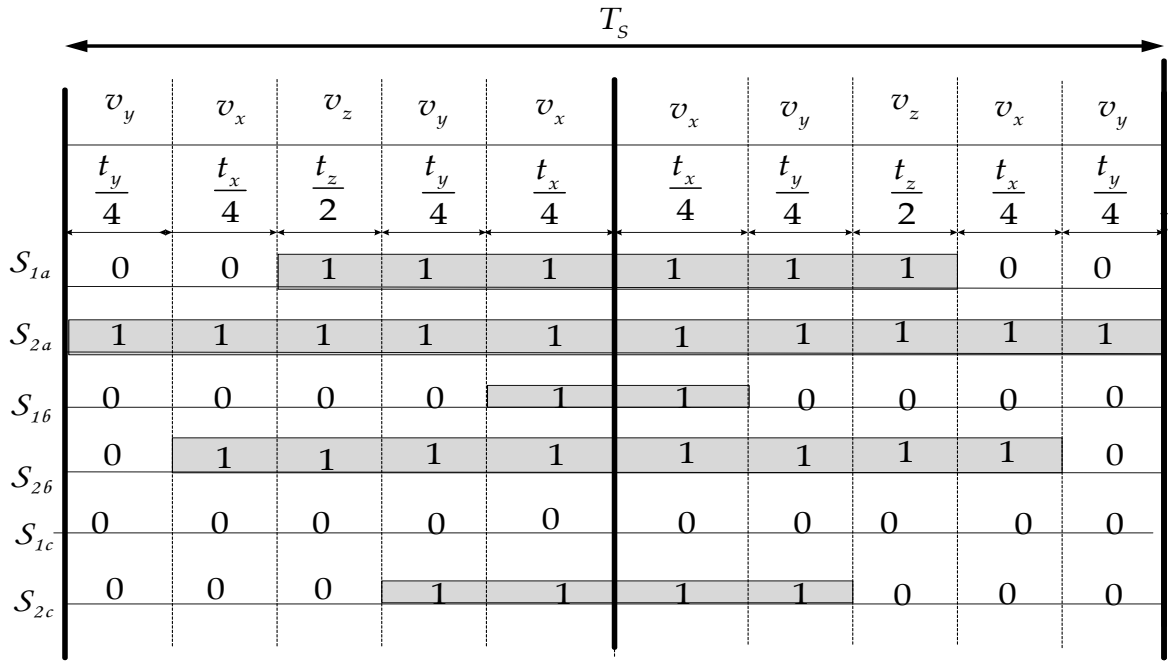
II.3.3. Pulses generation

In the same way as for the two-level SVM, the symmetrical switching sequence is also used for three-level SVM, figure (II.7) shows the pulses generation of all triangles located in the first sector.

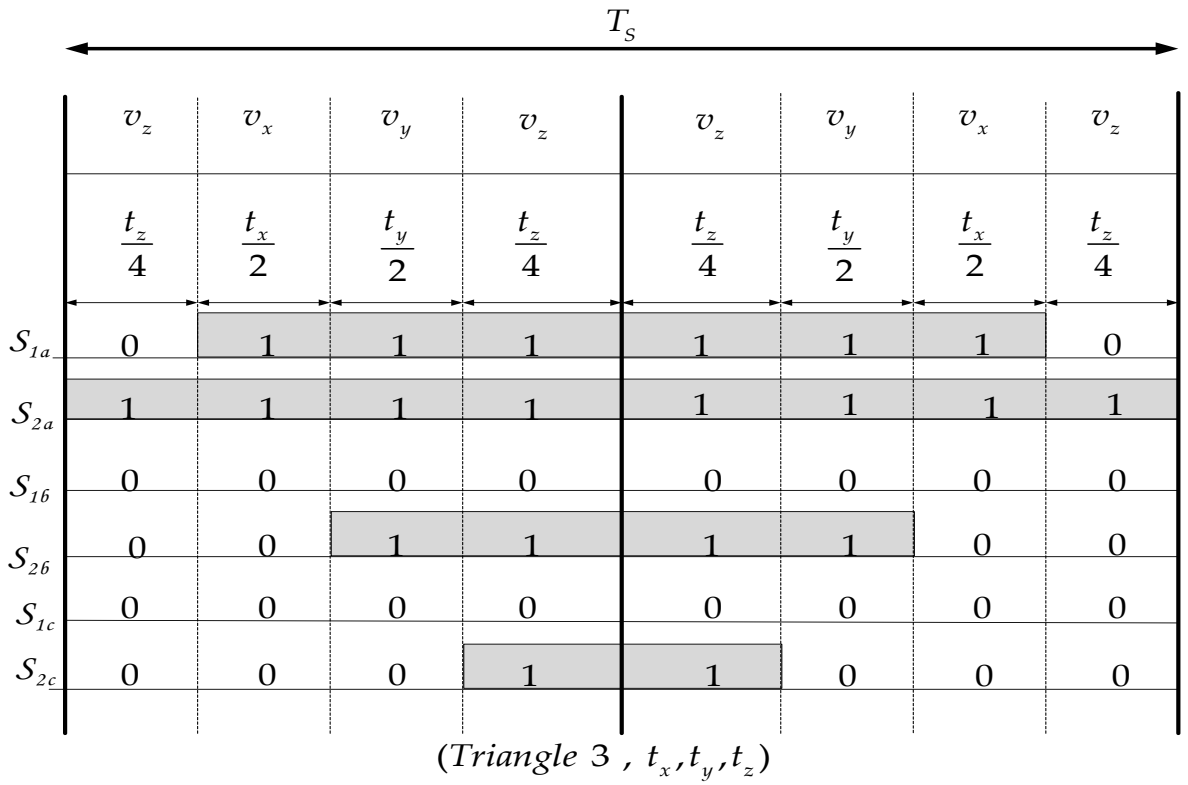
The generated pulses for all sectors are presented in figure (A.1) of appendix.



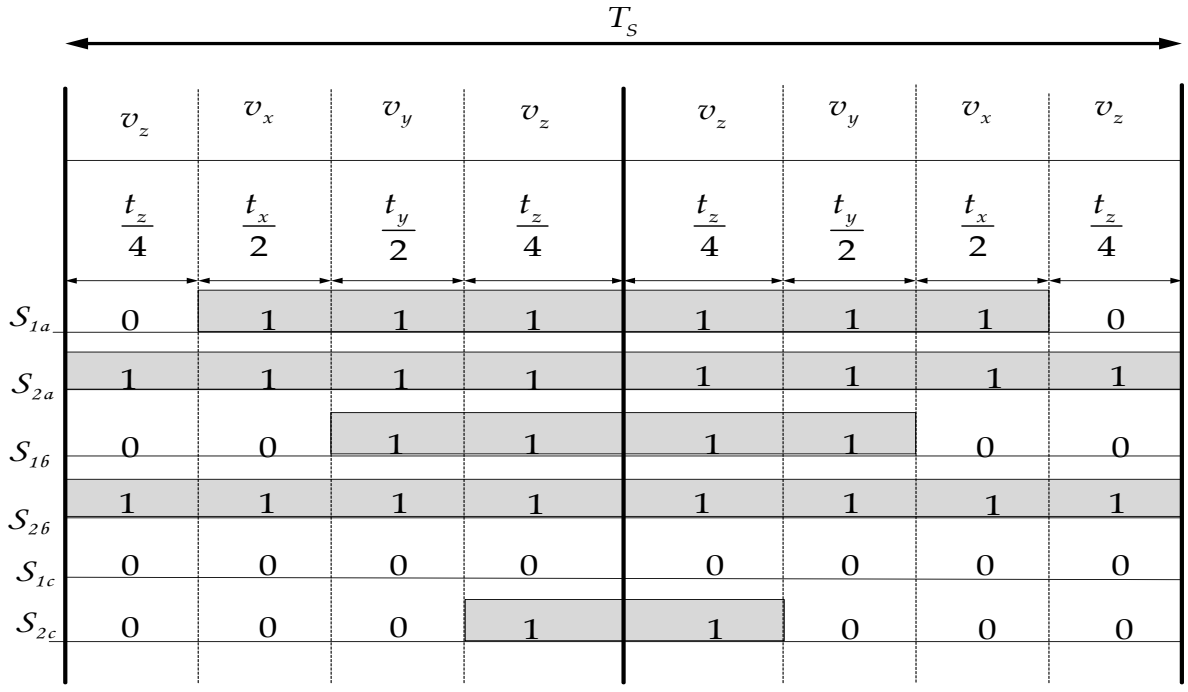
(*Triangle* 1 , t_x,t_y,t_z)



(*Triangle* 2 , t_x,t_y,t_z)



(*Triangle* 3 , t_x, t_y, t_z)



(*Triangle* 4, t_x, t_y, t_z)

Figure (II.7): Pluses generation of all triangles located in the first sector

Figure (II.8) summarizes all steps of the three-level SVM algorithm.

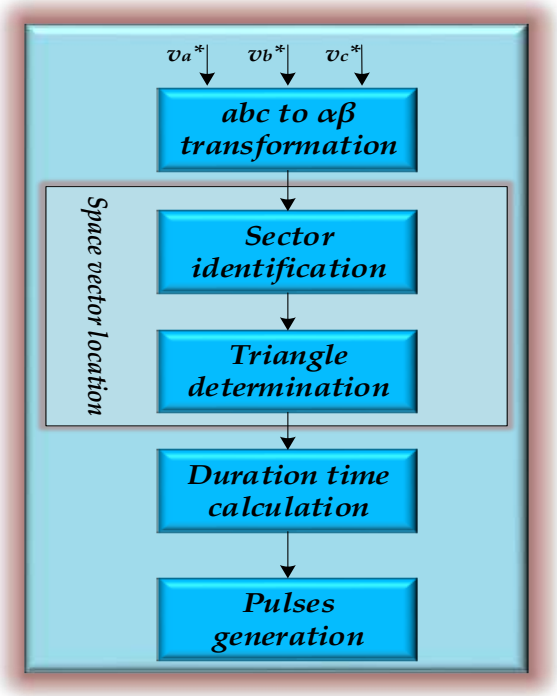


Figure (II.8): Three-level space vector modulation algorithm

II.4. Simulation Results

In this section, the SVM algorithm is verified by time-domain simulation for two and three-level inverters.

The inverter's load is an inductive load (R=500Ω, L=0.4H), the input DC voltage of the inverter is set to v_{dc} = 60 V, and the amplitude of the three-phase reference voltages is set to 30V.

Figures (II.9), (II.10) show the waveforms of the output voltage and load currents of two and three-level inverters respectively obtained with switching frequency 5 kHz. The same waveforms are presented with switching frequency 2 kHz and 1kHz respectively in figures (II.11), (II.12) and (II.13), (II.14).

As we can see, the quality of the voltage and currents waveforms is enhanced when the switching frequency is increased.

In the other side, comparing the performance obtained in the case of the three-level inverter with the two-level one, we find that under the same operating condition (same switching frequency), the three-level inverter produces a better output voltage and currents waveforms with less harmonics.

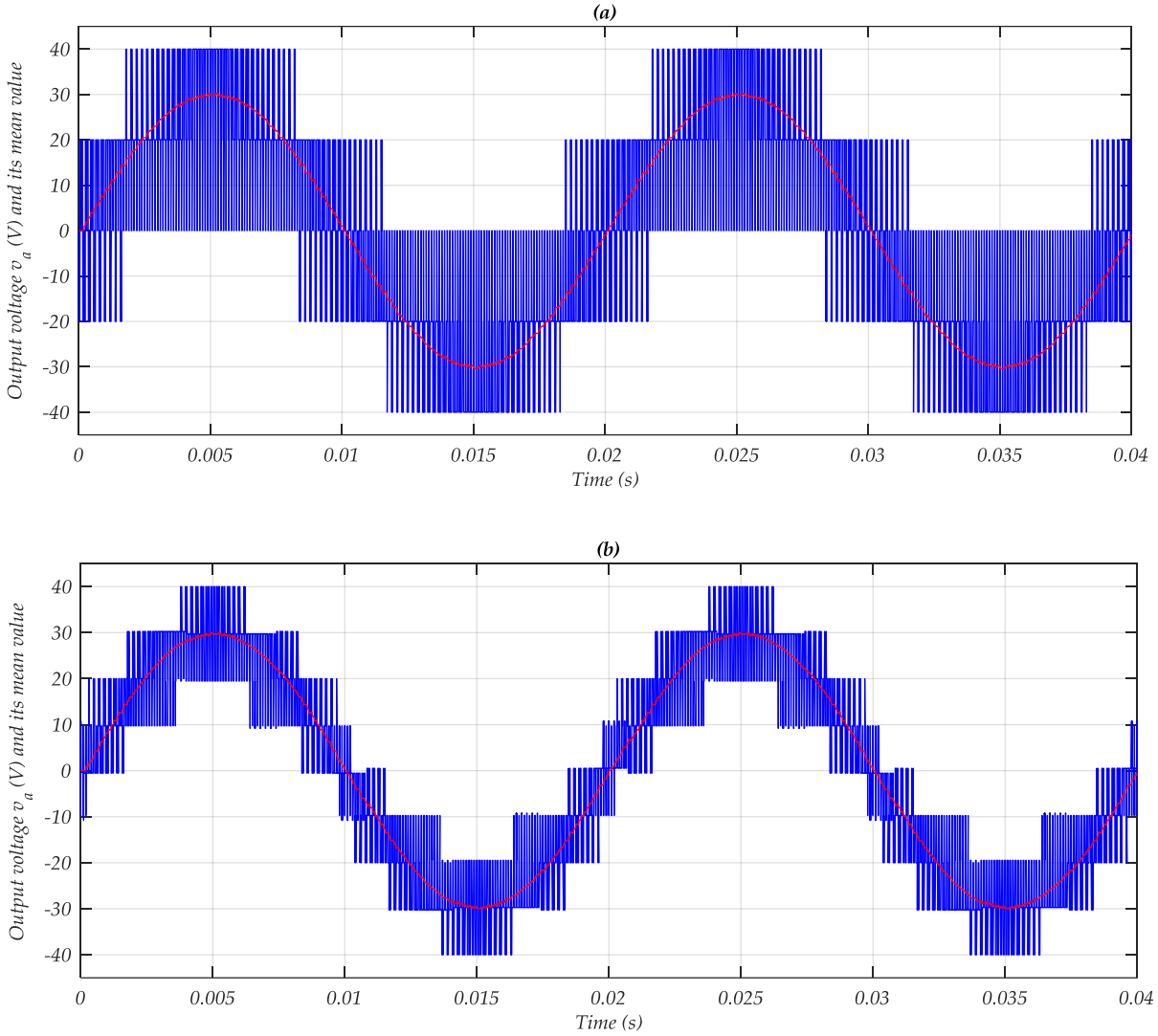


Figure (II.9): Output voltage of phase-a and its corresponding mean value under switching frequency 5 kHz, (a) for two-level inverter, (b) for three-level inverter

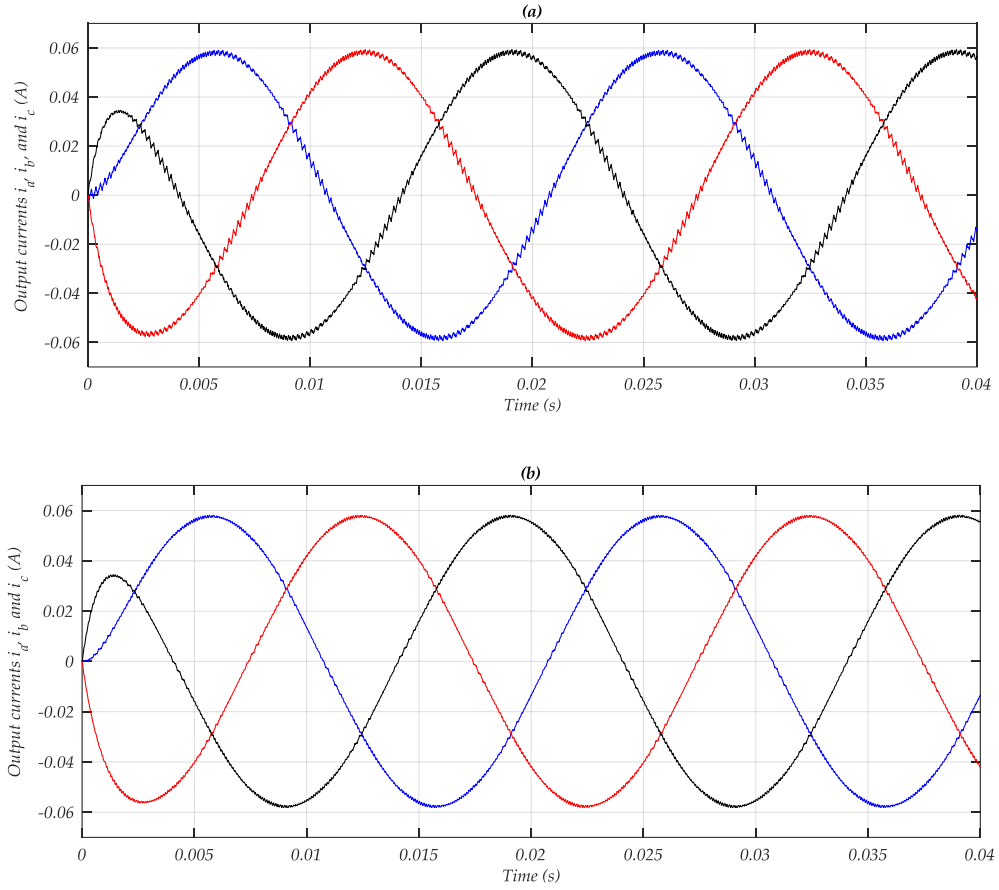
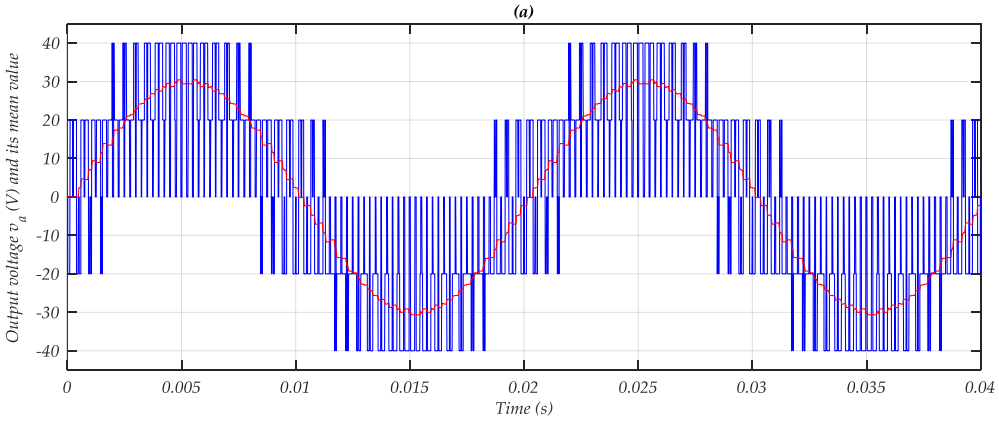


Figure (II.10): Load currents under switching frequency 5 kHz, (a) for two-level inverter, (b) for three-level inverter



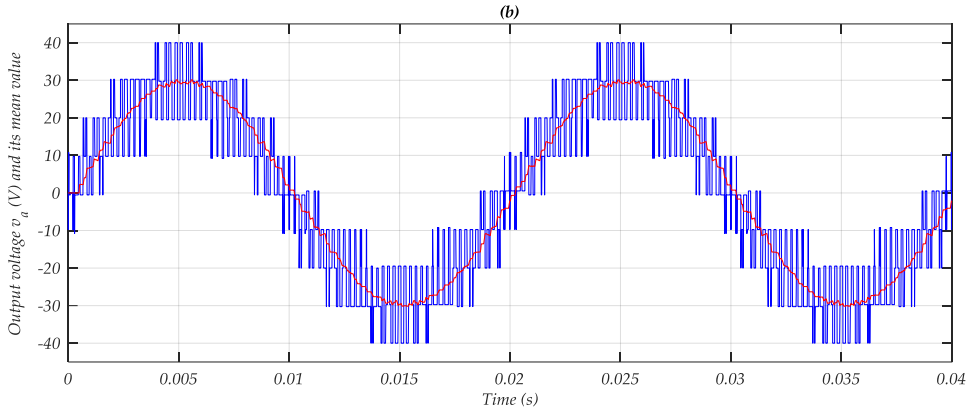


Figure (II.11): Output voltage of phase-a and its corresponding mean value under switching frequency 2 kHz, (a) for two-level inverter, (b) for three-level inverter

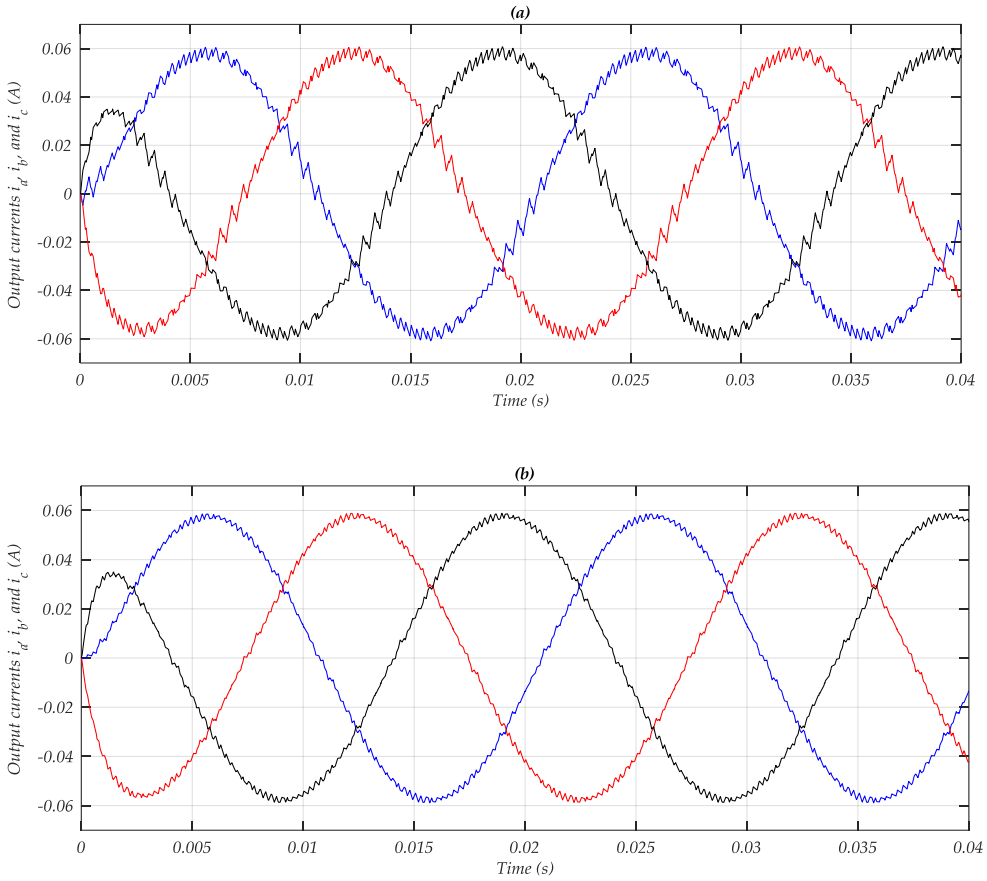


Figure (II.12): Load currents under switching frequency 2 kHz, (a) for two-level inverter, (b) for three-level inverter

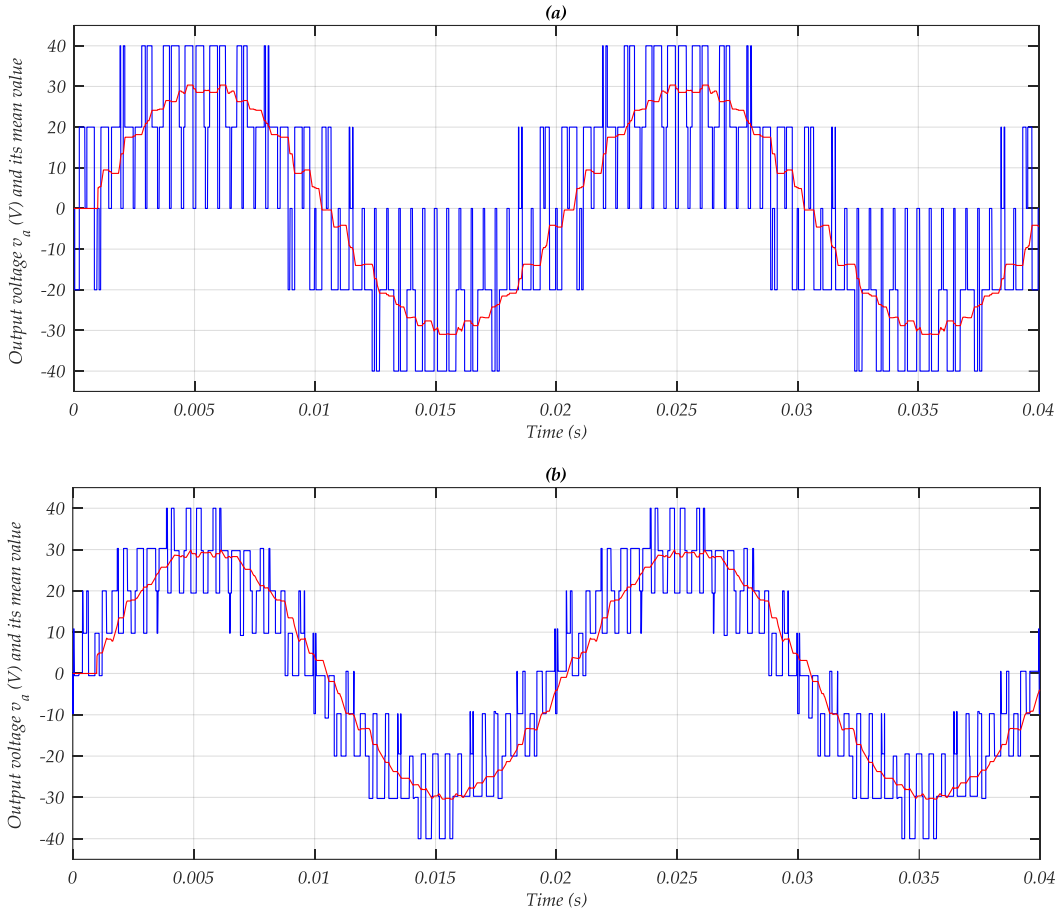
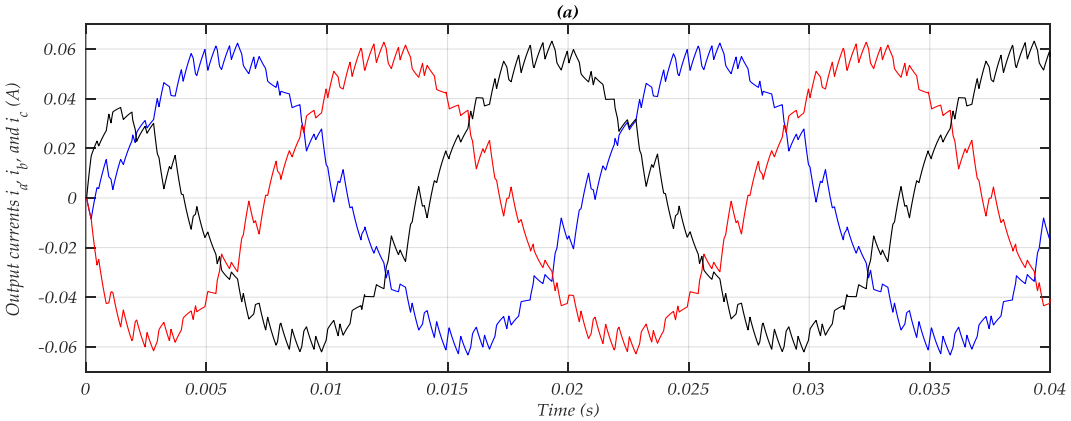


Figure (II.13): Output voltage of phase-a and its corresponding mean value under switching frequency 1 kHz, (a) for two-level inverter, (b) for three-level inverter



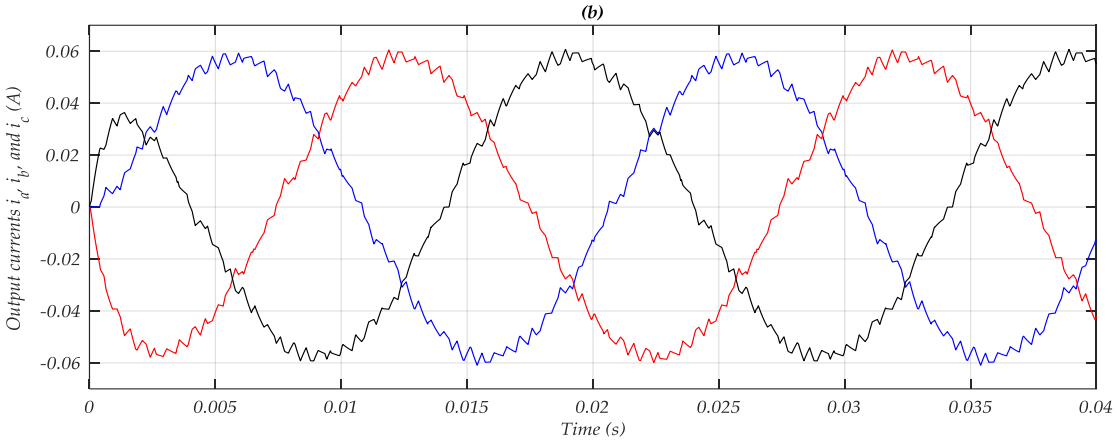


Figure (II.14): Load currents under switching frequency 1 kHz, (a) for two-level inverter, (b) for three-level inverter

Figure (II.15) illustrates the line-to-line voltage obtained with two and three-level inverters under switching frequency 5 kHz.

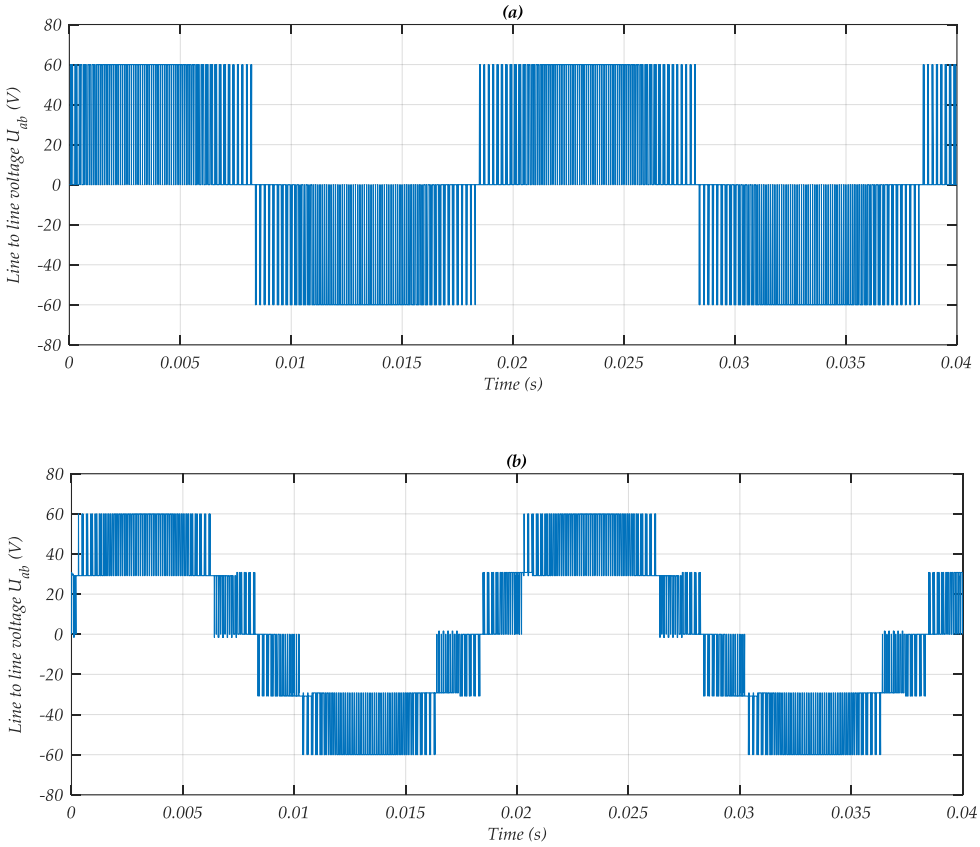


Figure (II.15): Line-to-line voltage, (a) for two-level inverter, (b) for three-level inverter

Table (II.4) shows the THD of the load current for different switching frequencies for two and three-level inverters, one notices well that the THD decreases remarkably with increase of the switching frequency. It can be concluded that the three-level inverter can operated with reduced switching frequency (1 kHz).

Table (II.4): Output current THD of two level, three-level and four leg inverters under different switching frequency

		Switching frequency (kHz)		
		1 kHz	2 kHz	5 kHz
Output current THD (%)	Two-level inverter	8.55%	5.24%	4.20%
	Three-level inverter	3.54%	1.13%	0.46%
	Four leg NPC inverter	14.15%	7.46%	3.00%

II.5. Conclusion

In this chapter, the space vector modulation for two and three-level inverters has been presented and analyzed. The algorithm of the space vector modulation has three main steps, reference voltage location, duration time calculation, and pulses generation. The algorithm in case of three-level is remarkably complicated compared with two-level one. Moreover, the simulation results show that the three-level inverter can produce a better quality of output voltages and currents with less harmonic compared to the conventional two-level inverter.

Chapter III

FPGA-Based control of three-phase three-level NPC inverter

III.1. Introduction

Two basic technologies, the digital signal processor (DSP), and the field programmable gate array (FPGA), have commonly been used for embedded applications [15]. Due to some special features such as fast processing speed, capability of parallel processing, and ability to provide multiple PWM generators according to the converter requirements, the FPGA technology may be an excellent choice for medium-voltage multilevel converters [16]. Although several design techniques are available for the development of FPGA-based switching controller, most of them require special software, which increases not only the developmental time but also the cost of the controller. In this chapter, a fully digital switching controller is developed for a 3-phase 3-level converter. The GPS40B120U IGBTs are used to develop a prototype multilevel converter, and a Xilinx Zynq-7020 FPGA is used to develop the switching controller.

The most common software such as the MATLAB/Simulink- and Xilinx ISE-based alternative design technique is used, which may reduce the developmental time and cost of the switching controller. The simulation results serve as a preliminary validation of the proposed design technique, which will be finally verified by the experimental results. The developed switching scheme can be used for any multilevel converter configurations with very little change in the software environment. Moreover, the proposed design and implementation techniques may be useful for designing any other modern power converter's switching controller.

III.2. DSP and FPGA technology

III.2.1. Digital Signal Processing (DSP) Technology

The DSP has a fixed hardware configuration, which is the hardware of the basic functions of many signal processing algorithms. The DSP technology is a fast microprocessor, which has much flexibility with different features. The DSP technology is typically programmed in C/C++ or with assembly language for performance. This technology is well suited to extremely complex mathematical tasks, with conditional processing. However, the performance of DSP technology is limited by the clock rate, and the number of useful operations per clock. For example, the TMS320C6201 can achieve 400 million multiplications per second with two multipliers and 200-MHz clock [17]. Figure (III.1) shows a photograph of DSP by Texas Instruments.

Figure (III.1): Photograph of a DSP

III.2.2. Field Programmable Gate Array (FPGA) Technology

An FPGA (Field Programmable Gate Array) is a programmable logic device that consists of a large number of simple logic elements (LEs). The FPGA is programmed using a Very-high-speed integrated Hardware Description Language (VHDL), which programs the connections between the individual LEs to create logical functions (i.e., digital hardware) [18]. Figure (III.2) shows a photograph of Xilinx FPGA.

Figure (III.2): Photograph of an FPGA by Xilinx

The main limitations of FPGA technology are the number of LEs and signal propagation delay. Advancements in FPGA technologies have increased the number of the available LEs and reduced the propagation delay. Recent FPGAs have more multipliers. For example, Xilinx Spartan-6 XC6SLX150T has 180 multipliers that can operate at 100 MHz, which gives 18,000 million multiplications per second [19]. In comparison with the DSP technology, the advanced FPGA technology gives 10–100 times faster processing speed. The yearly growth of FPGA capabilities compared to the traditional DSP is depicted in figure (III.3) [20]. The most important performance criteria of modern controllers are use of high performance control algorithms, easy to modify the control strategy and parameters, fully integrated single device controllers, low cost as well as implementation time, and high reliability and accuracy. In this regard, recent studies have shown that FPGA could be an appropriate alternative over DSP for many applications.

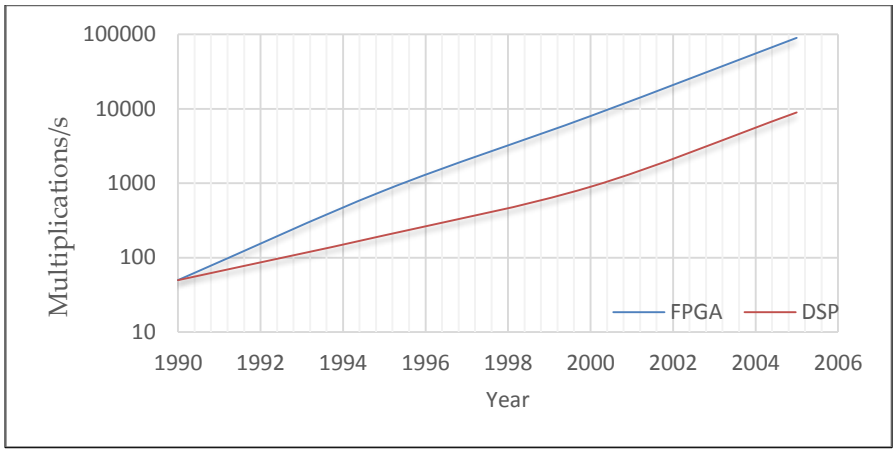


Figure (III.3): Multiplications per second of Texas instruments DSP and Altera FPGA

The FPGA may run all the operations in parallel with the clock signal. The capability of parallel processing of the FPGA provides the opportunity to the switching controller to update all gate signals simultaneously, Unlike the DSP which runs a sequential program in its microprocessor [20]. In most cases, the processing time is independent of the number of converter levels. Therefore, the FPGA technology is a natural choice for the control of multilevel converters. A comparison between the FPGA and the DSP technology is summarized in the table (III.1).

Table (III.1): A comparison between the DSP and the FPGA technology

Performance indicators	***Options***	
	DSP	***FPGA***
More than a few MHz sample rates	Hard to handle	Easy to handle
Programming language	Standard C/C++	VHDL
More than 30 Mb/s data rate	Hard to handle	Easy to handle
Conditional operations	Easy to implement	Hard to implement
Use of floating point	Easy to implement	Hard to implement
PWM output channel	Limited (about six pairs)	Can be configured as required
Parallel processing	Serial implementation	Serial/parallel implementation

III.3. Structure of FPGA

III.3.1. Internal structure of FPGA

FPGA consists of an array of configurable logic blocks (CLBs), surrounded by programmable I/O blocks, and connected with programmable interconnect by a switch matrix shown in figure (III.4).

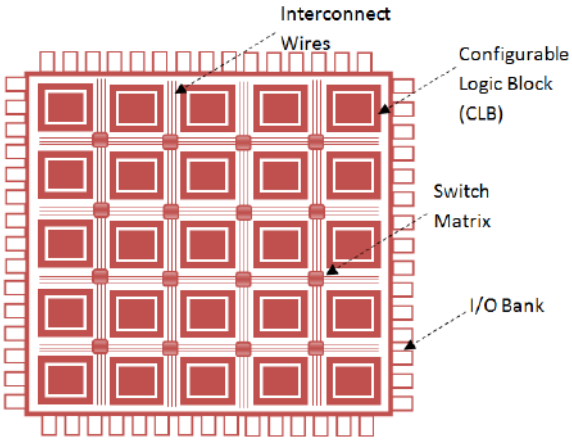


Figure (III.4): Internal structure of FPGA

Each logic cell can independently take on any one of a limited set of personalities. The individual cells are interconnected by a matrix of wires and programmable switches. A user's design is implemented by specifying the simple logic function for each cell and selectively closing the switches in the interconnect matrix. Complex designs are created by combining these basic blocks to create the desired circuit [21].

III.3.2. Design flow of a Xilinx FPGA

The simplified design flow of an FPGA-based system is shown in figure (II.5). The left portion of the flow is the refinement and programming process, in which a system is transformed from an abstract textual HDL description to a device cell-level configuration and then downloaded to the FPGA device. The right portion is the validation process, which checks whether the system meets the functional specification and performance goals. The major steps in the flow are:

1- ***Design Entry***: The first step in creating a new design is to specify it's structure and functionality. This can be done either by writing an HDL model using some text editor (VHDL or Verilog) or drawing a schematic diagram using schematic editor.

2- ***Design Synthesis:*** Next step in the design process is to transform design specification (RTL design specification) into a more suitable representation (gate-level representation) that can be further processed in the later stages in the design flow.

3- ***Design Implementation:*** The implementation process consists of three smaller processes: translate, map, and place and route. The translate process merges multiple design files to a single netlist. The map process, which is generally known as technology mapping, maps the generic gates in the netlist to FPGAs logic cells and IOBs. The place and route process, which is generally known as placement and routing, derives the physical layout inside the FPGA chip. It places the cells in physical locations and determines the routes to connect various signals. In the Xilinx flow, static timing analysis, which determines various timing parameters, such as maximal propagation delay and maximal clock frequency, is performed at the end of the implementation process.

4- ***Design Verification:*** is very important step in design process. A verification is comprised of seeking out problems in the HDL implementation in order to make it compliant with the design specification. A verification process reduces to extensive simulation of the HDL code. Design Verification is usually performed using two approaches: Simulation and Static Timing Analysis.

5- ***Generate Programming File:*** this option runs Xilinx bitstream generation program, to create a bitstream file that can be downloaded to the device.

6- ***Programming****:* - Xilinx ISE offers Open iMPAC programmer option that uses the native in-system device programming capabilities that are built into the Xilinx ISE. Hardware manager uses the output from the Generate Programming File process to configure your target device.

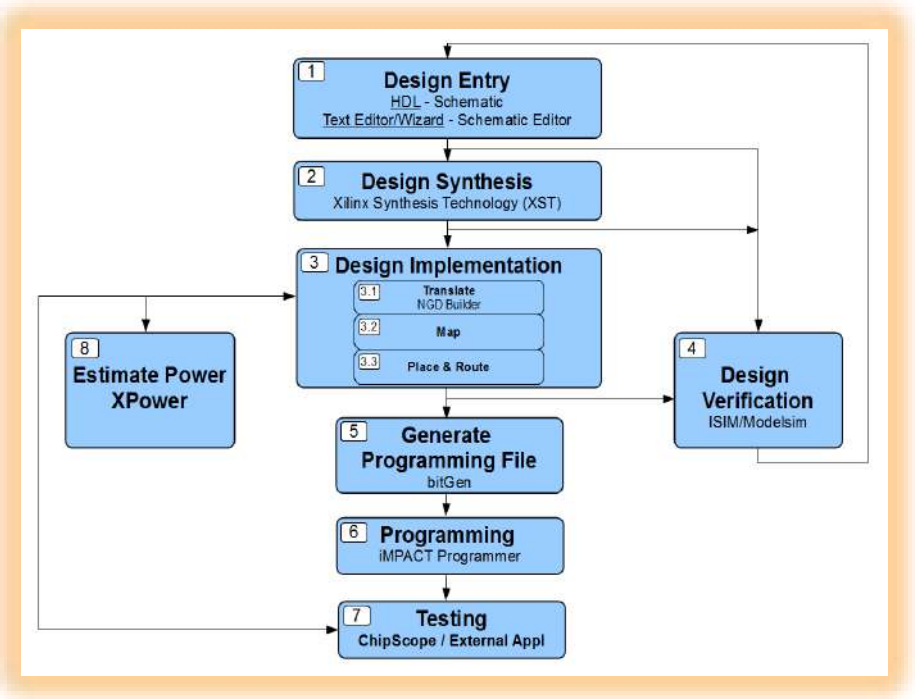


Figure (III.5): Xilinx FPGA design flow

Figure (III.6) shows Xilinx ZedBoard Zynq-7020 development board that was used to implement the three-level SVM.

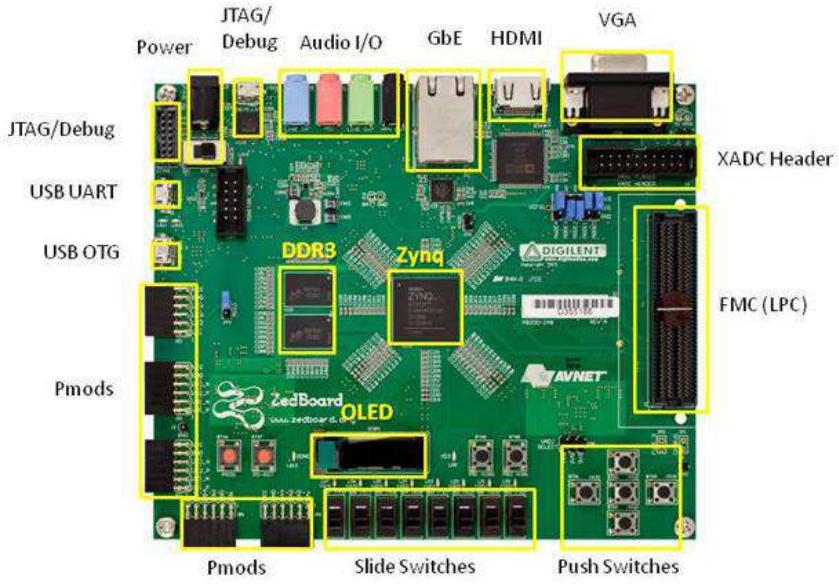


Figure (III.6): ZedBoard Zynq-7020 Development Board

The ZedBoard is an evaluation and development board based on the Xilinx Zynq-7020 Extensible Processing Platform. Combining a dual Corex-A9 Processing System (PS) with 85,000 Series-7 Programmable Logic (PL) cells, the Zynq-7020 EPP can be targeted for broad use in many applications. The ZedBoard's robust mix of on-board peripherals and expansion capabilities make it an ideal platform for both novice and experienced designers [22]. The figure (III.7) shows the Zynq bank pin assignments on the ZedBoard followed by the detailed I/O connections.

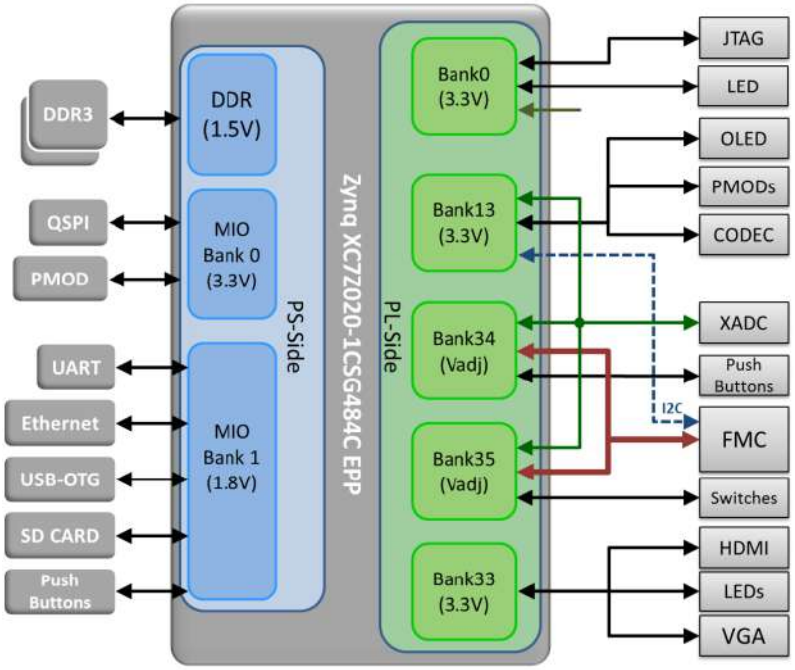


Figure (III.7): Xilinx- Zynq Z7020 CSG484 Bank Assignments

The features provided by the ZedBoard consist of:

- ❖ Xilinx® XC7Z020-1CSG484CES EPP
  - ➢ Primary configuration = QSPI Flash
  - ➢ Auxiliary configuration options
    - Cascaded JTAG
    - SD Card
- ❖ Memory
  - ➢ 512 MB DDR3 (128M x 32)

- 256 Mb QSPI Flash

❖ Interfaces

- USB-JTAG Programming using Digilent SMT1-equivalent circuit
  - Accesses PL JTAG
  - PS JTAG pins connected through PS Pmod
- 10/100/1G Ethernet
- USB OTG 2.0
- SD Card
- USB 2.0 FS USB-UART bridge
- Five Digilent Pmod™ compatible headers (2x6) (1 PS, 4 PL)
- One LPC FMC
- One AMS Header
- Two Reset Buttons (1 PS, 1 PL)
- Seven Push Buttons (2 PS, 5 PL)
- Eight dip/slide switches (PL)
- Nine User LEDs (1 PS, 8 PL)
- DONE LED (PL)

❖ On-board Oscillators

- 33.333 MHz (PS)
- 100 MHz (PL)

❖ Display/Audio

- HDMI Output
- VGA (12-bit Color)
- 128x32 OLED Display
- Audio Line-in, Line-out, headphone, microphone

❖ Power

- On/Off Switch
- 12 V @ 5 A AC/DC regulator

❖ Software

- ISE® WebPACK Design Software
- License voucher for ChipScope™ Pro locked to XC7Z020

III.4. Implementation of three-level SVM based on FPGA

In this thesis, the VHDL-code-based behavioral models of different SVM blocks are designed and synthesized using the Project Navigator tool of the Xilinx ISE Design Suite 14.7 software. Figure (III.8) shows the RTL schematic of control unit for three-level SVM, as we can see, there are three inputs:

- Clock (clk);
- Reset;
- Select of switching frequency (Choice).

And 12 gate pulses for three-level inverter as outputs.

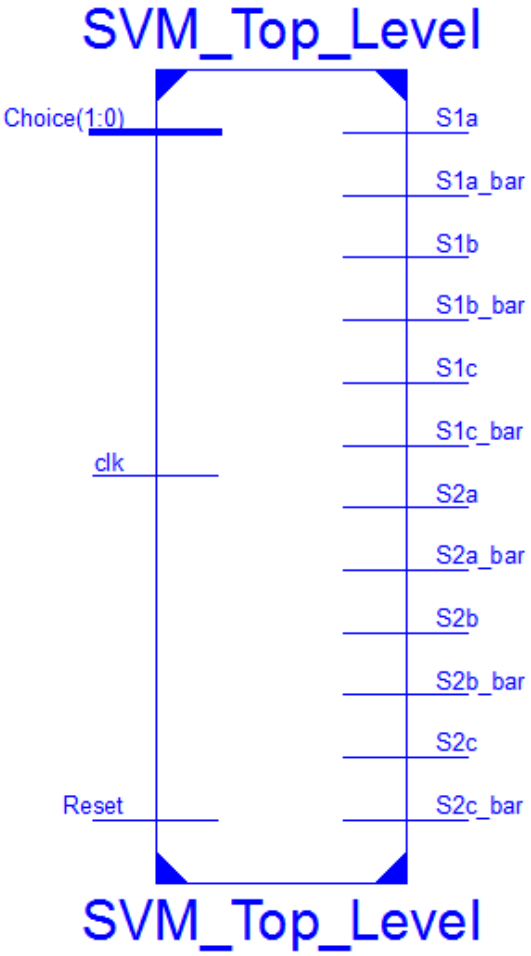


Figure (III.8): RTL schematic of three-level SVM

The RTL schematic of three-level SVM shown in figure (III.8) contains 12 VHDL modules as presented in figure (III.9):

The clock source of ZedBoard FPGA is 100 MHz, therefore, the clock divider should be used to reduces the clock frequency in order to obtain the reference voltages frequency of 50 Hz.

In order to generate the 50 Hz three-phase voltage output waveform, three reference signals with 120° phase-shifted from each other are needed. A VHDL-code-based program is used to create the Look Up Tables (LUT), which contains the sine references that makes the control circuit totally digital and integrated.

The block coordinate transformation converts the reference voltages v_a, v_b and v_c to two signals v_α and v_β, these signals are required to find the sector number (Sector identification block), and to identified the triangle number (Triangle identification block).
The switching time block uses four signals, v_α, v_β, sector number and triangle number to calculate the switching times of the adjacent switching vectors t_1, t_2 and t_3.
The inputs of on-off times block are switching times t_1, t_2 and t_3, sector number and triangle number, while their outputs are on-off switching times that are used to create the gate signals in the next block (Find pulses).

The implemented three-level SVM can operate with different switching frequency thanks to the block of select of switching frequency. This latter can change the switching frequency according to its input (choice). When the choice = "00", the switching frequency is 1 kHz, when "01" the switching frequency is 2kHz, for the remaining combinations of the choice, the switching frequency is 5kHz.

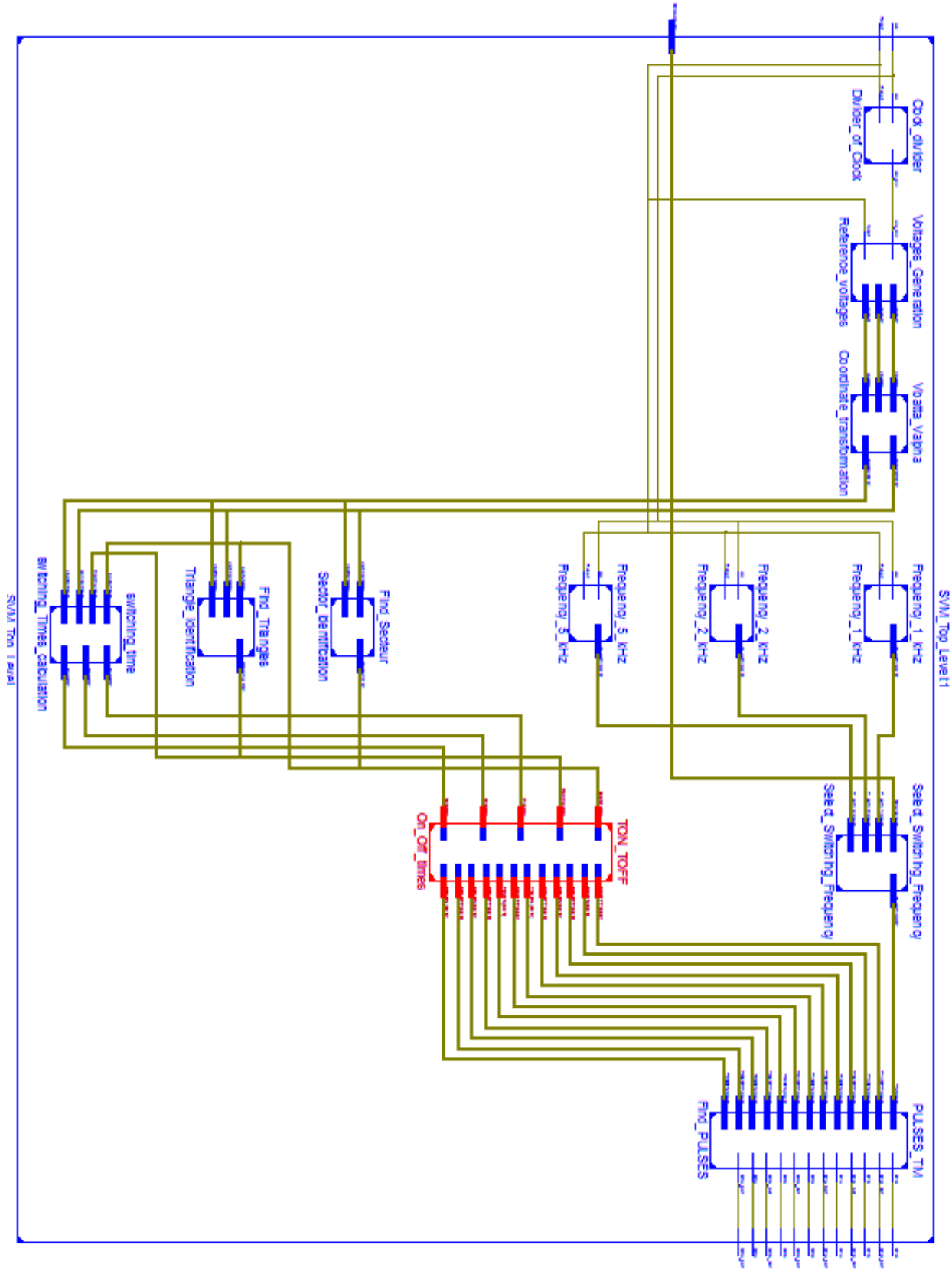


Figure (III.9): RTL schematic inside of three-level SVM

III.4.1. Dead time creation

Since the turn-off time of power devices is usually longer than its turn-on time, and therefore, an appropriate delay time named (dead-time) must be inserted between these two gating signals of the two complementary switches to avoid the short circuit. Therefore, a programmable delay-time is introduced in the designed SVM architecture, this dead time effect can be modeled in the VHDL language by introducing a delay time some microseconds usually 1 to 4 µs. The following figure shows the dead time between a tow complementary signals in the first leg.

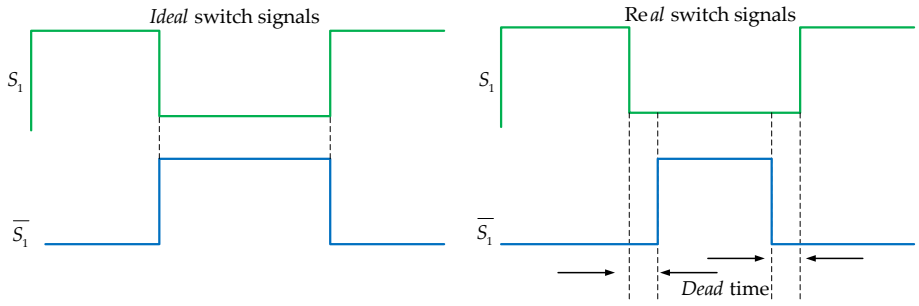


Figure (III.10): Dead time insertion

III.5. Block diagram of hardware model

Figure (III.11) shows the block diagram representation of the hardware model that is divided in tow main part, control and power parts.

The control part contains:

- FPGA board, which is used to generate the desired switching signals;
- Driver circuit, which is used to give necessary isolation and to amplify the signals for complete turn on of IGBT switches.

The power part includes:

- DC power supply;
- Three-level inverter;
- Three phase inductive load.

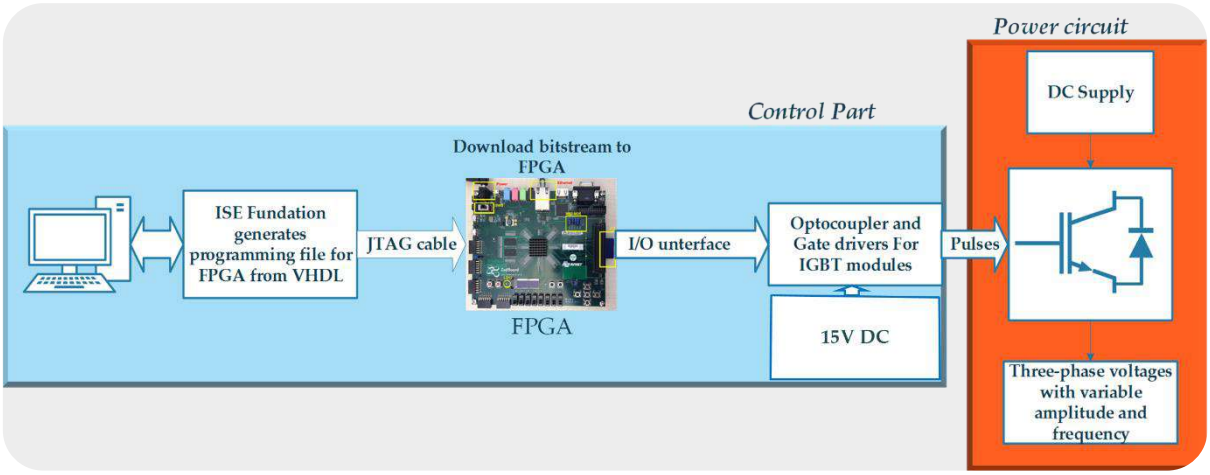


Figure (III.11): Block diagram of FPGA based three-level inverter

III.5.1. Control part

1- ***Output pins box:*** Output pins box is shown in figure (III.12) is connected directly to the output of FPGA, to make the connection of FPGA easy with other circuits.

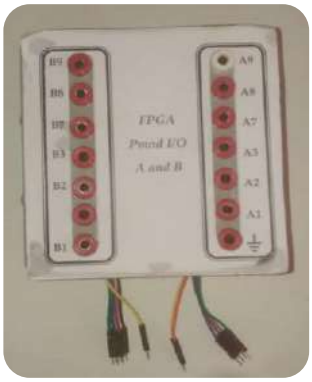


Figure (III.12): Output Pmod FPGA

2- ***Insulator gate driver circuit***: The output voltage of the FPGA is 3.3 V, which is not enough to drive the IGBTs of the inverter. Therefore, the HCPL-3120 Drive Optocoupler is used to increase the voltage level to 15 V, and to provide a negative voltage (-5V) to turn off the IGBT when the output voltage coming from FPGA is zero (see figure (III.13)).

This driver is also used to isolate the FPGA board from the power circuit.

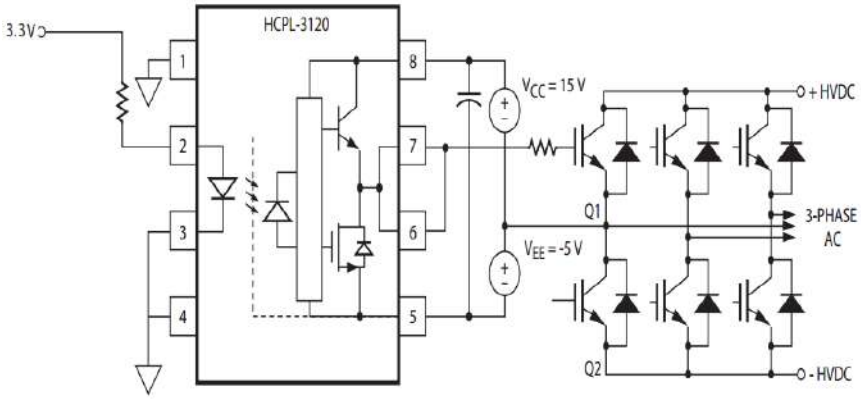
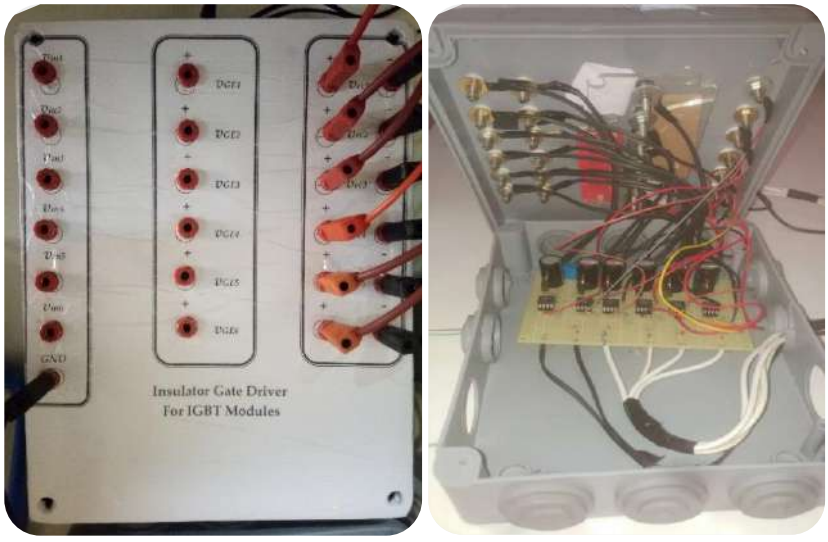


Figure (III.13): HCPL-3120 Typical Application Circuit with Negative IGBT Gate Drive

Figure (III.14) shows the driver box from inside and outside, which consist of six pins (+ and -) connected to 15 V DC supply box, six pins with GND connected to FPGA board and six pins (+15 V and -5 V) output of the driver to turn on and turn off the IGBTs.



(a) (b)

Figure (III.14): Insulator Gate Driver box for IGBT Modules,
(a): from outside, (b): from inside

Figure (III.15) shows the schematic circuit of one driver for one IGBT that composed by the following components:

- HCPL-3120 Drive Optocoupler;

- Two capacitors C_1 and C_2 of 1 mF/63 V and 100 nF/35 V respectively;
- Voltage regulator L7815;
- Two resistances R_1 and R_2 of 300 Ω and 10 Ω.
- DC voltage of 5V.

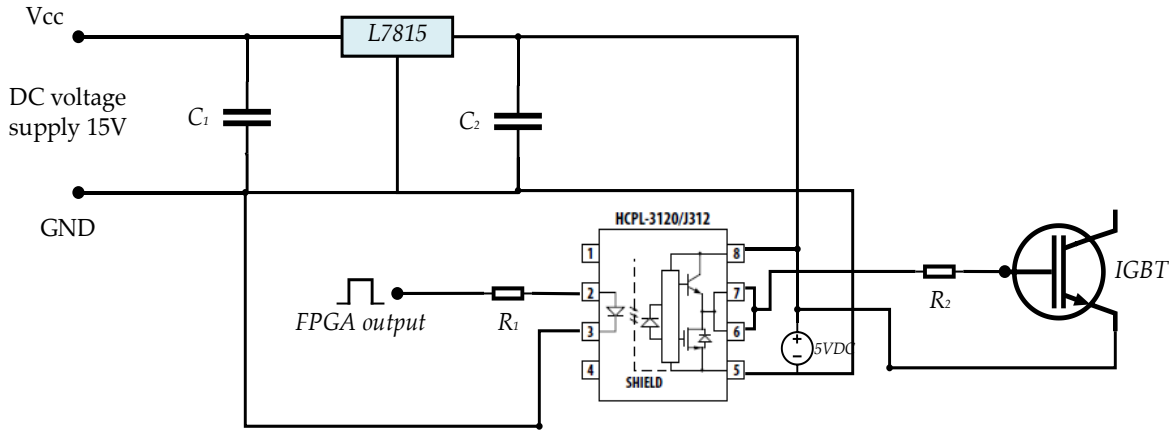
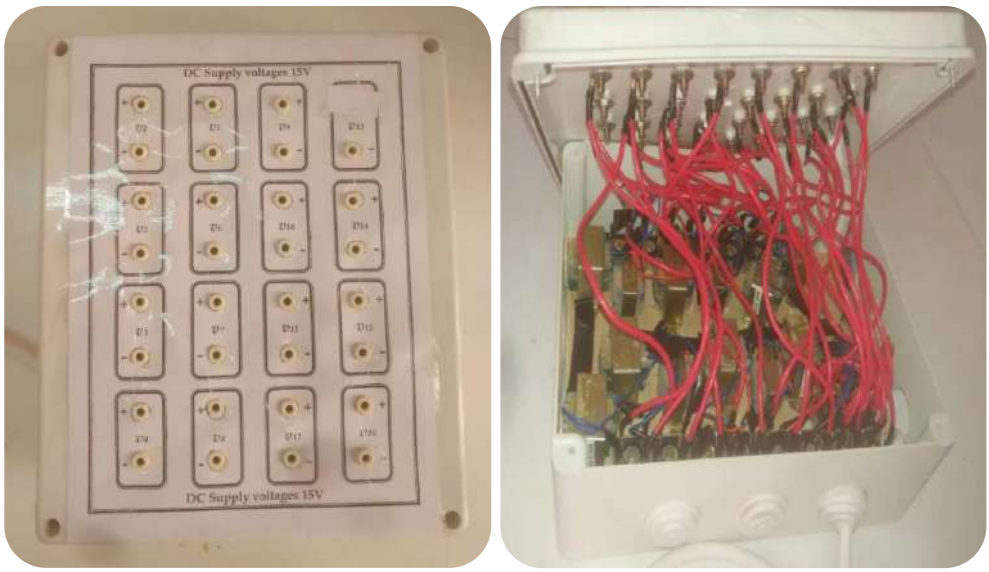


Figure (III.15): Schematic circuit of one driver for one IGBT

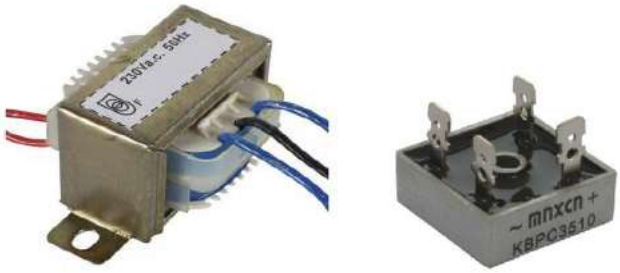
3- ***DC Power supply 15V***: As shown in figure (III.16) 16 DC voltage are used in order to feed two driver boxes (12 driver for three-level inverter).



(a) (b)

Figure (III.16): The box of DC Supply voltages 15 V, (a): from outside, (b): from inside

This power supply contains 16 transformers 220/12 V and 16 H-Bridge rectifier (KBPC3510) see figure (III.17).



(a) (b)

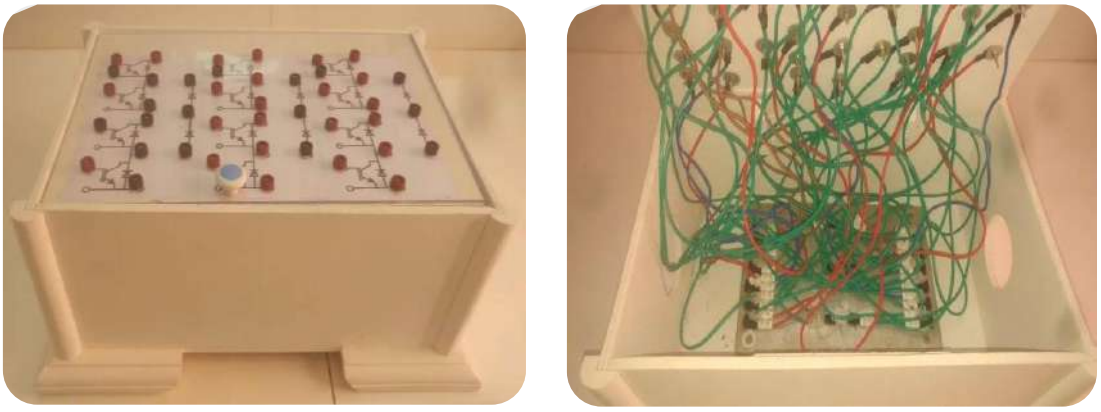
Figure (III.17): DC power supply components, (a): transformers 220/12 V, (b): H-Bridge rectifier (KBPC3510)

III.5.2. Power part

The used power components are described as follow:

1. ***Three-level inverter***: contains two components:

- 12 Insulated Gat Bipolar Transistor (IGBT) IRGPS40B120U.
- 6 clamping diodes BY459X-1500.



(a) (b)

Figure (III.18): Three-level inverter, (a): From outside (b): From inside.

2. ***Three-phase inductive load***: R = 500 Ω and L = 0.4 H (see figure (III.19)).

3. ***DC power supply 60 V***: is used to feed the three-level inverter (see figure (III.19)).

III.6. Experimental results

The experimental setup of the switching controller for the three-level inverter system is illustrated in figure (III.19). The gate pulses from the driver circuit can be used to switch the switching devices.

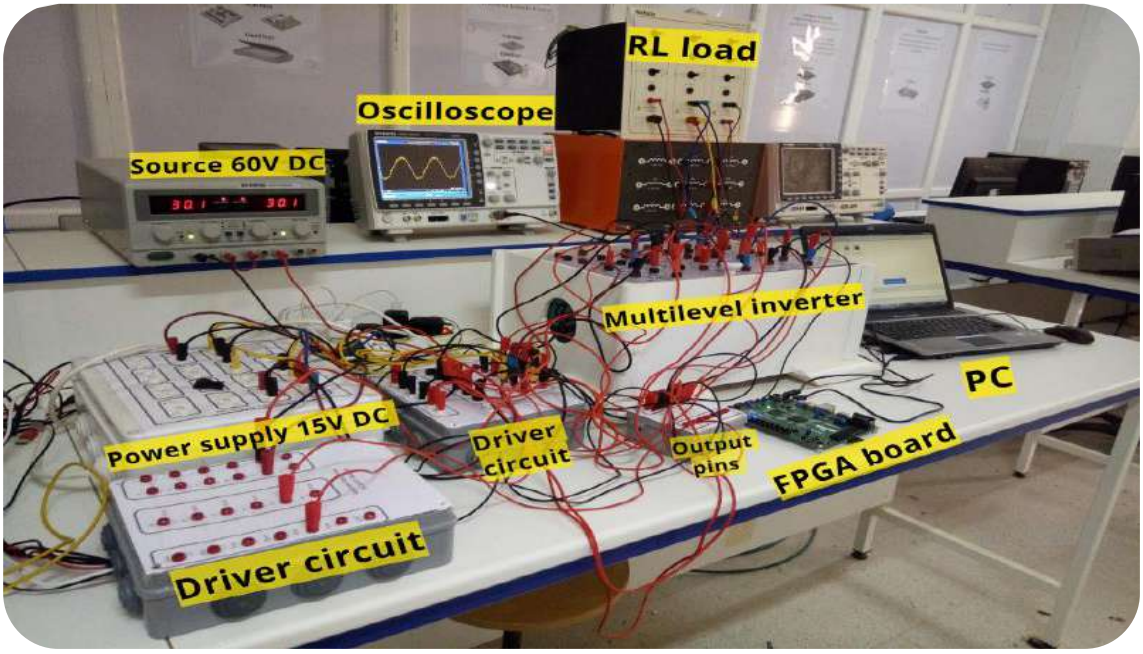


Figure (III.19): Photograph of the complete experimental hardware setup

To observe experimental results of GWINSTEK GDS2202A Oscilloscope 200 MHz is used. The inverter's load is an inductive load (R = 500 Ω, L = 0.4 H), the input DC voltage of the inverter is set to v_{dc} = 60 V, and the amplitude of the three-phase reference voltages is set to 30V with frequency of 50 Hz.

The gate pulses from FPGA and driver circuit are illustrated in figure (III.20). The measured switching frequency of the switching signals is 5 kHz, which well matches the theoretical result.

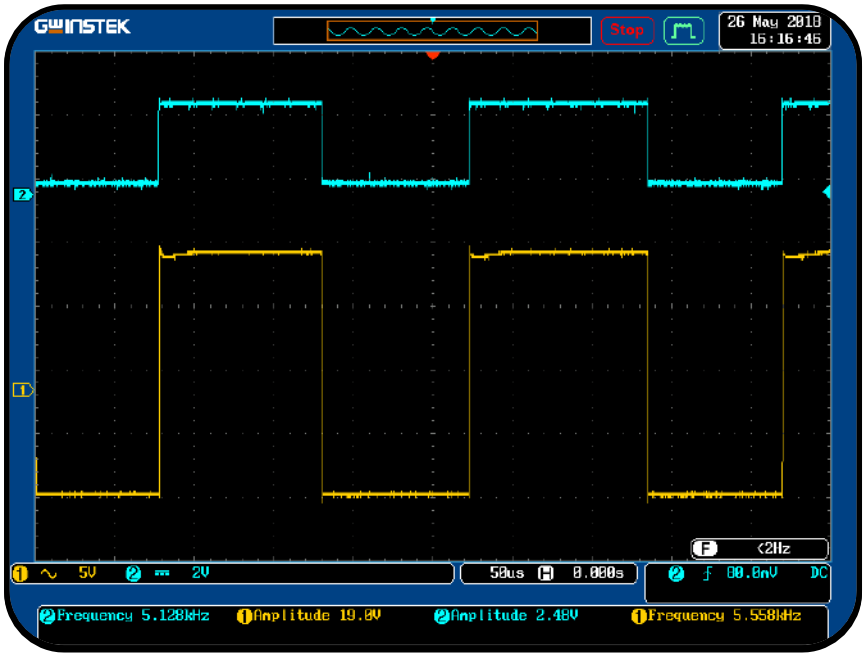


Figure (III.20): Measured gate pulses from FPGA and driver circuit

Figure (III.21) presents a gate pulse and its corresponding complementary. It is clear that the operation with dead time is successfully achieved, the switching devices remain off before one turns on, which ensures the safe operation of both switching devices (the dead time is set to 4 µs).

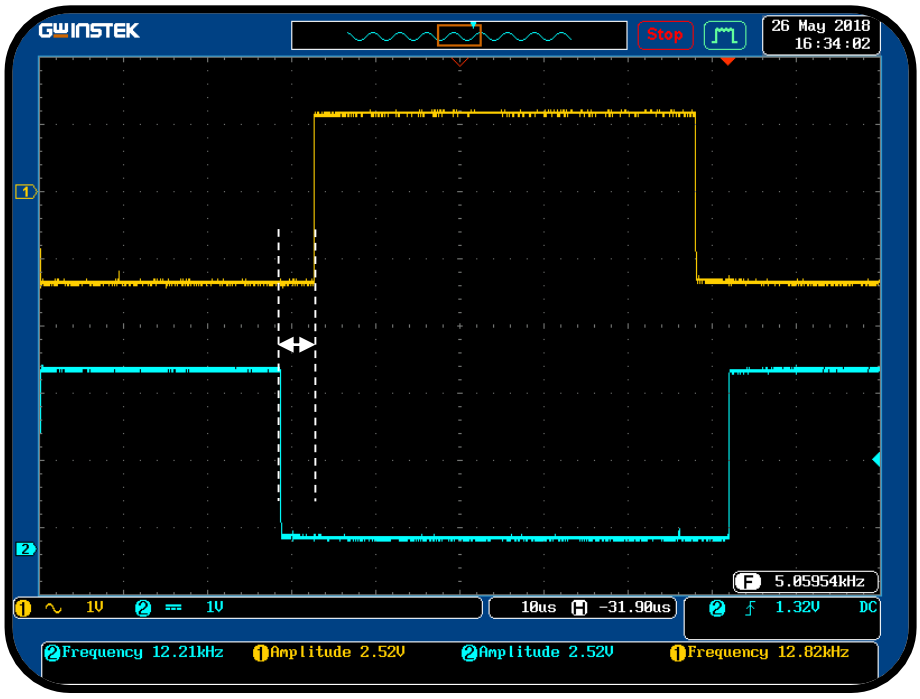
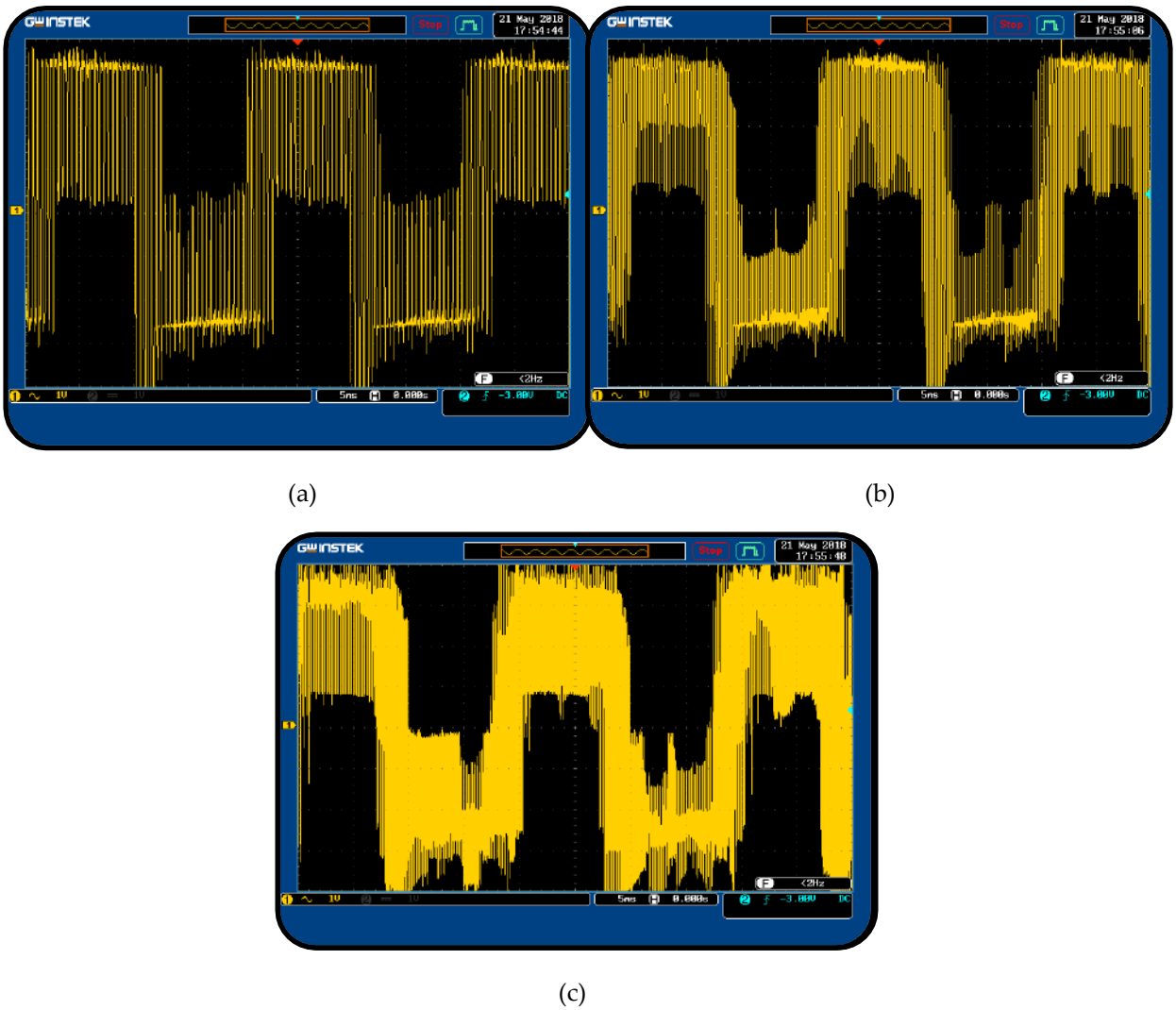


Figure (III.21): Measured gate pulses of a switching device and its corresponding complementary

Figures (III.22) show the waveforms of the line to middle point voltage v_{ao} of three-level inverter obtained with switching frequency 1 kHz, 2 kHz and 5 kHz respectively.

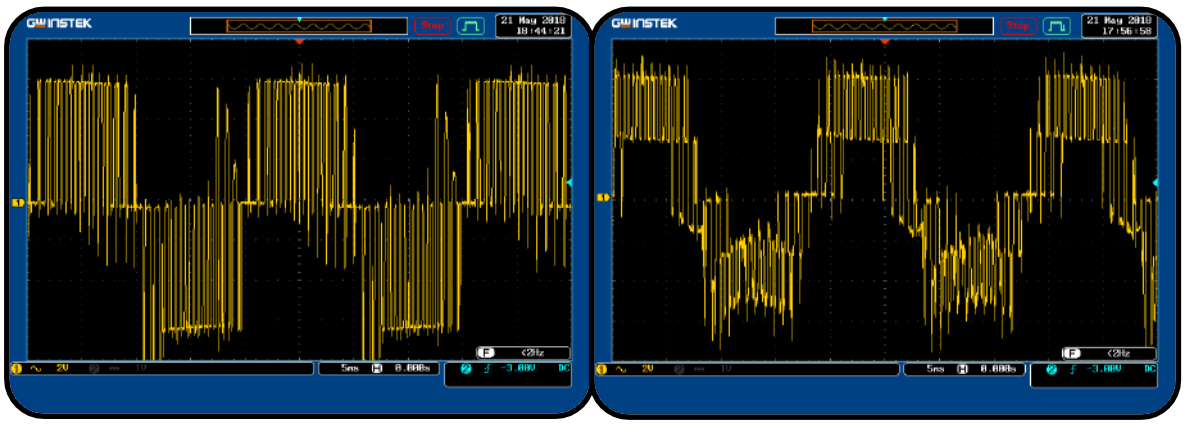


(a) (b)

(c)

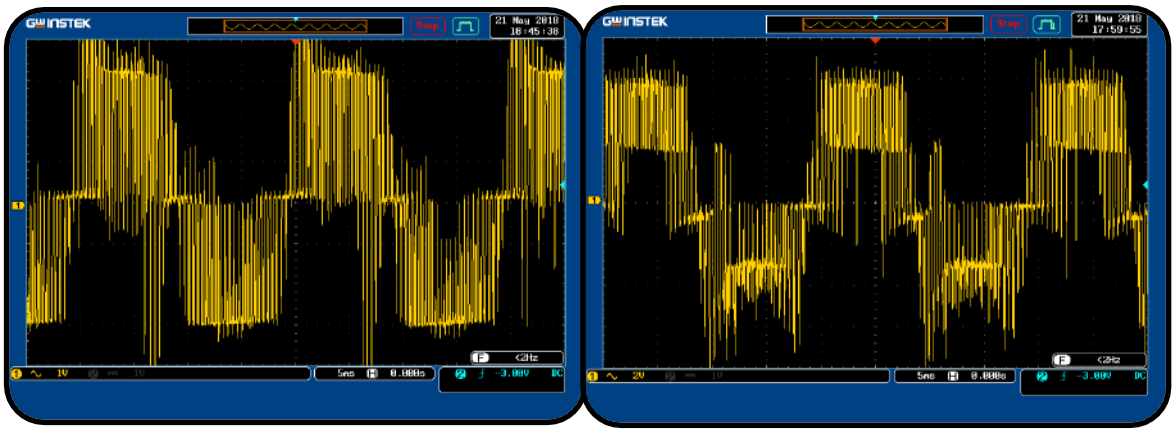
Figure (III.22): Experimental results of line to middle point voltage v_{ao} of the three-level inverter under switching frequency, (a): 1 kHz, (b): 2 kHz, (c): 5 kHz

Figures (III.23), (III.24), (III.25) show experimental results of the output line-to-line voltage U_{ab} of two and three-level inverters obtained with different switching frequency (1 kHz, 2 kHz and 5kHz). It is clear that the quality of the voltage waveform obtained with the three-level inverter is better compared to that obtained with two-level inverter. These results are highly consistent with MATLAB/Simulink results.



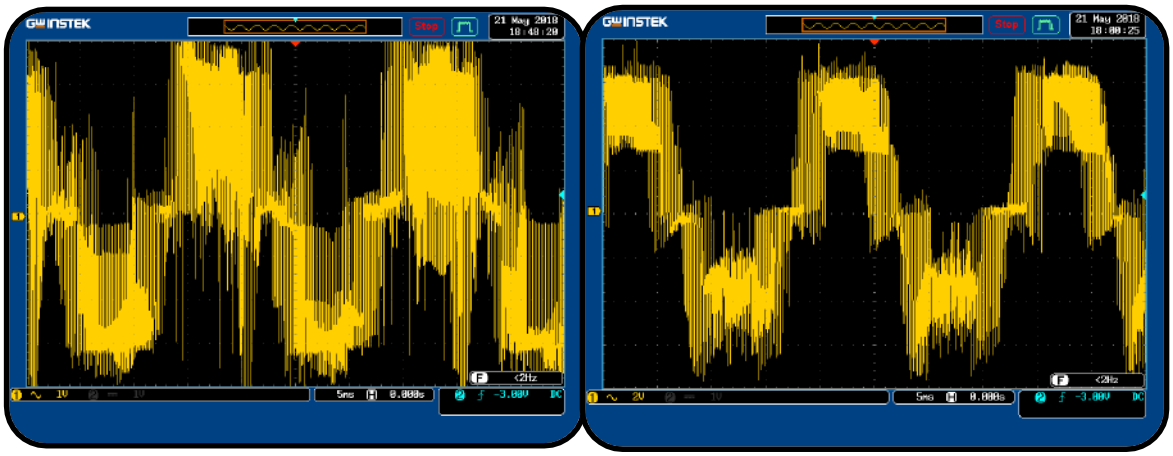
(a) (b)

Figure (III.23): Experimental results of one phase line-to-line voltage U_{ab} under switching frequency 1 kHz, (a): for two-level inverter, (b): for three-level inverter



(a) (b)

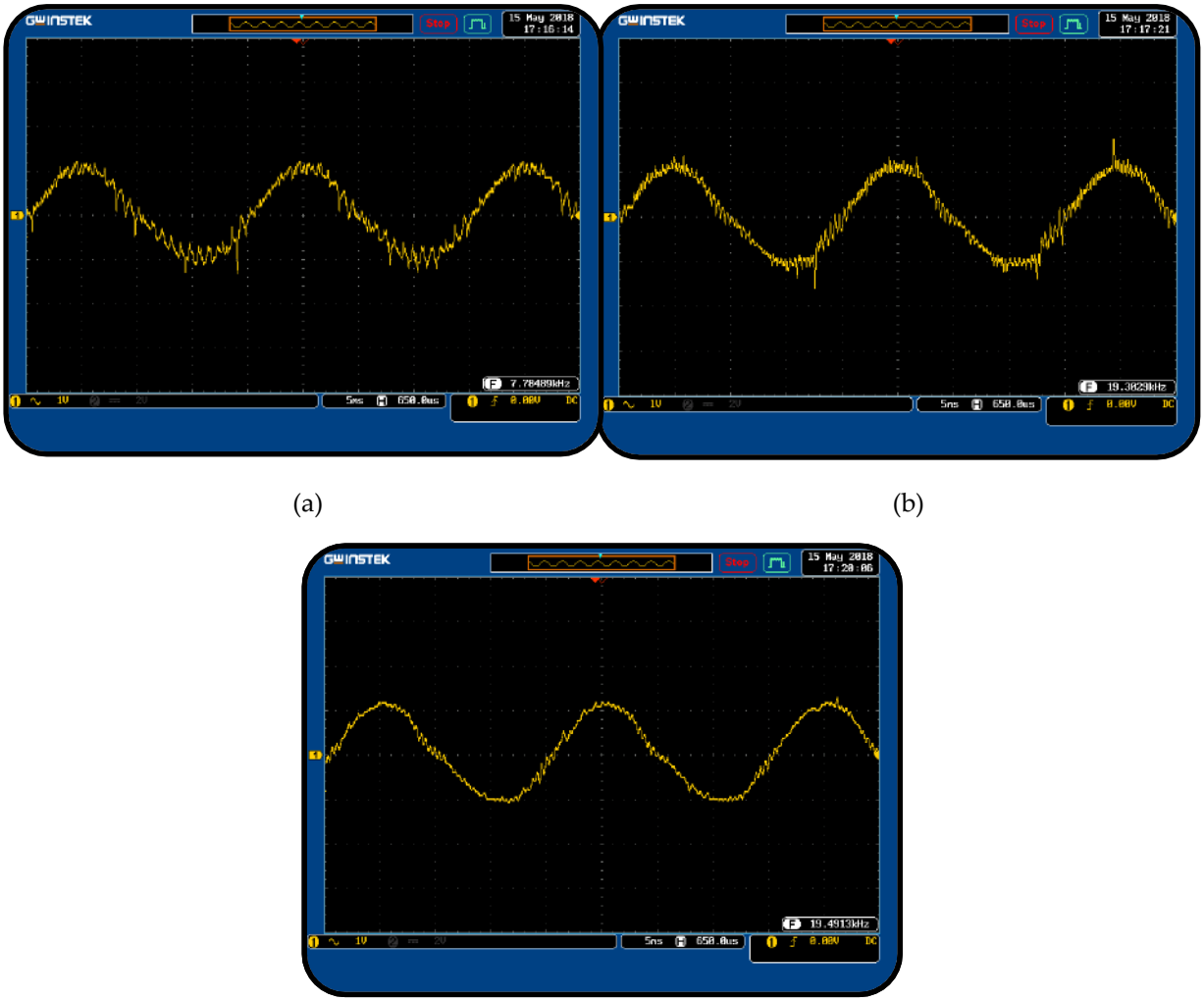
Figure (III.24): Experimental results of one phase line-to-line voltage U_{ab} under switching frequency 2 kHz, (a): for two-level inverter, (b): for three-level inverter



(a) (b)

Figure (III.25): Experimental results of one phase line-to-line voltage U_{ab} under switching frequency 1 kHz, (a): for two-level inverter, (b): for three-level inverter

Figures (III.26) show the waveforms of the load currents of two level inverter obtained with switching frequency 1 kHz, 2 kHz and 5 kHz. As we can see, the quality of load current waveform is enhanced when the switching frequency is increased.



(a) (b)

(c)

Figure (III.26): Experimental results of the load current of two-level inverter under different switching frequency, (a): 1 kHz, (b): 2 kHz, (c) 5 kHz

III.7. Conclusion

This chapter has described the design and implementation of space vector modulation of the three-level inverter based on FPGA. The FPGA may be the natural choice because of its high-speed operation and capacity to handle multiple PWM signals. An integrated fully digital switching controller has been developed for a three-phase three-level inverter system using an FPGA development board. The experiment results have been carried out successfully and show that under the same operating condition, the three-level inverter produces a better output voltage waveforms compared to two-level inverter.

General conclusion

Multilevel inverters are suitable for high-voltage applications because of their ability to synthesize output voltage waveforms with a better harmonic spectrum and attain higher voltages with a limited maximum device rating.

At the first of this thesis, a comprehensive analysis of the two and three-level inverter, including the inverter configurations, basic principles, and mathematical modeling have been provided. This makes the three-level inverter has a more degree of freedom to synthesize an output voltage and current with less harmonics.

In order to control both two and three-level inverters, the space vector modulation has been selected due to the advantages they can offer compared to other modulation techniques. The algorithm of the space vector modulation has three main steps, reference voltage location, duration time calculation, and pulses generation. The algorithm in case of three-level is remarkably complicated compared with two-level one. Moreover, the simulation results show that the three-level inverter can produce a better quality of output voltages and currents with less harmonic compared to the conventional two-level inverter.

In other side, a real-time approach for the implementation of space vector modulation for three-level inverter has been performed and described. The experiment results have been carried out successfully, which are consistent with the analytical waveforms and simulation results.

The following topics can be suggested for the future works:

- Using the three-level inverter as an active power filter.
- Extension of SVM technique to multilevel inverters (more than three-level),
- Association of the DC capacitor voltages balancing algorithm to the SVM strategy.
- Using high-level synthesis tools for Xilinx FPGAs.

References

[1] D. Soto and T. C. Green, "A comparison of high-power converter topologies for the implementation of FACTS controllers," *IEEE Trans. Ind. Electron.*, vol. 49, no. 5, pp. 1072–1080, Oct. 2002.

[2] Fang Zheng Peng, "A generalized multilevel inverter topology with self voltage balancing," *IEEE Trans. Ind. Appl.*, vol. 37, no. 2, pp. 611–618, 2001.

[3] Jae Hyeong Seo, Chang Ho Choi, and Dong Seok Hyun, "A new simplified space-vector PWM method for three-level inverters," *IEEE Trans. Power Electron.*, vol. 16, no. 4, pp. 545–550, Jul. 2001.

[4] T. Bruckner and D. G. Holmes, "Optimal Pulse-Width Modulation for Three-Level Inverters," *IEEE Trans. Power Electron.*, vol. 20, no. 1, pp. 82–89, Jan. 2005.

[5] S. K. Mondal, B. K. Bose, V. Oleschuk, and J. O. P. Pinto, "Space vector pulse width modulation of three-level inverter extending operation into overmodulation region," *IEEE Trans. Power Electron.*, vol. 18, no. 2, pp. 604–611, Mar. 2003.

[6] P. M. Menghal and A. J. Laxmi, "Real time control of electrical machine drives: A review," in *2010 International Conference on Power, Control and Embedded Systems*, 2010, pp. 1–6.

[7] A. Fratta, G. Griffero, and S. Nieddu, "Comparative analysis among DSP and FPGA-based control capabilities in PWM power converters," in *30th Annual Conference of IEEE Industrial Electronics Society, 2004. IECON 2004*, vol. 1, pp. 257–262.

[8] M. M. Kumar1, N.Karthini, and M.Revathy, "Transistor Clamped Cascaded H-BridgeMultilevel Inverter Fed Induction Motor Drive," *Int. J. Innov. Res. Sci. Eng. Technol.*, vol. 3, no. 1, pp. 732–737, 2014.

[9] J. M. MAZA-ORTEGA, E. ACHA, S. GARCÍA, and A. GÓMEZ-EXPÓSITO, "Overview of power electronics technology and applications in power generation transmission and distribution," *J. Mod. Power Syst. Clean Energy*, vol. 5, no. 4, pp. 499–514, Jul. 2017.

[10] P. Boonchiam and N. Mithulananthan, "Diode-clamped Multilevel Voltage Source Converter Based on Medium Voltage DVR," *Int. J. Electr. Power Energy Syst. Eng.*, pp. 62–67, 2008.

[11] S. Khomfoi and L. M. Tolbert, "Multilevel Power Converters," in *Power Electronics Handbook*, Elsevier, 2007, pp. 451–482.

[12] H. Hu, W. Yao, and Z. Lu, "Design and implementation of three-level space vector PWM IP core for FPGAs," *IEEE Trans. Power Electron.*, vol. 22, no. 6, pp. 2234–2244, 2007.

[13] M. Bouzidi, A. Benaissa, and S. Barkat, "Hybrid direct power/current control using feedback linearization of three-level four-leg voltage source shunt active power filter," *Int. J. Electr. Power Energy Syst.*, vol. 61, pp. 629–646, 2014.

[14] E. A. R. Engku Ariff, O. Dordevic, and M. Jones, "A Space Vector PWM Technique for a Three-Level Symmetrical Six-Phase Drive," *IEEE Trans. Ind. Electron.*, vol. 64, no. 11, pp. 8396–8405, 2017.

[15] M. R. Islam, Youguang Guo, and Jianguo Zhu, "FPGA-based control of modular multilevel converters: Modeling and experimental evaluation," in *2015 International Conference on Electrical & Electronic Engineering (ICEEE)*, 2015, pp. 89–92.

[16] M. R. Islam, Y. Guo, and J. Zhu, "A High-Frequency Link Multilevel Cascaded Medium Voltage Converter for Direct Grid Integration of Renewable Energy Systems," *IEEE Trans. Power Electron.*, vol. PP, no. 99, p. 1, 2013.

[17] Data sheet of FIXED-POINT DIGITAL SIGNAL PROCESSOR VelociTI " http://www.ti.com/product/%20tms320c6424"

[18] Data sheet of Spartan-6 Family Overview Summary of Spartan-6 FPGA Features,"https://www.xilinx.com/products/silicon-devices/fpga/spartan-6.html "

[19] S. Jose, "FPGAs rapidly replacing high-performance DSP capability," *DSP-FPGA.COM MAGAZINE*, 2018. [Online]. Available: http://dsp-fpga.com/article-id/?2051. [Accessed: 28-Feb-2007].

[20] M. R. Islam, Y. Guo, and J. Zhu, "Multiple-input multiple-output medium frequency-link based medium voltage inverter for direct grid connection of photovoltaic arrays," *2013 Int. Conf. Electr. Mach. Syst.*, no. October, pp. 202–207, 2013.

[21] Danesh Tavana, Wilson Yee, Steve Young, and Bradly Fawcett, "Logic Block and Routing Considerations for a New SRAM-Based FPGA Architecture," IEEE Custom Integrated Circuits Conference, 1995, pp. 511-514.

[22] Avnet, "Zynq™ Evaluation and Development Hardware User's Guide," 2018. [Online]. Available: https://reference.digilentinc.com/reference/programmable-logic/zedboard/reference-manual. [Accessed: 01-Aug-2012].

Appendix

Table (A.1): Duration time intervals of all triangles of all sectors

Sector 1	Triangle 1	$\begin{bmatrix} t_x \\ t_y \end{bmatrix} = \begin{bmatrix} \sqrt{6} & -\sqrt{2} \\ 0 & 2\sqrt{2} \end{bmatrix} \begin{bmatrix} v_\alpha^* \\ v_\beta^* \end{bmatrix} \frac{T}{v_{dc}}$	Triangle 2	$\begin{bmatrix} t_x \\ t_y \end{bmatrix} = \begin{bmatrix} \frac{\sqrt{6}}{2} & \frac{-3\sqrt{2}}{2} \\ \sqrt{6} & 2\sqrt{2} \end{bmatrix} \begin{bmatrix} v_\alpha^* \\ v_\beta^* \end{bmatrix} \frac{T}{v_{dc}}$
	Triangle 3	$\begin{bmatrix} t_x \\ t_y \end{bmatrix} = \begin{bmatrix} 0 & 2\sqrt{2} \\ \sqrt{6} & -\sqrt{2} \end{bmatrix} \begin{bmatrix} v_\alpha^* \\ v_\beta^* \end{bmatrix} \frac{T}{v_{dc}}$	Triangle 4	$\begin{bmatrix} t_x \\ t_y \end{bmatrix} = \begin{bmatrix} \sqrt{6} & -\sqrt{2} \\ -\frac{\sqrt{6}}{2} & \frac{3\sqrt{2}}{2} \end{bmatrix} \begin{bmatrix} v_\alpha^* \\ v_\beta^* \end{bmatrix} \frac{T}{v_{dc}}$
Sector 2	Triangle 1	$\begin{bmatrix} t_x \\ t_y \end{bmatrix} = \begin{bmatrix} \sqrt{6} & \sqrt{2} \\ -\sqrt{6} & \sqrt{2} \end{bmatrix} \begin{bmatrix} v_\alpha^* \\ v_\beta^* \end{bmatrix} \frac{T}{v_{dc}}$	Triangle 2	$\begin{bmatrix} t_x \\ t_y \end{bmatrix} = \begin{bmatrix} \sqrt{6} & 0 \\ -\sqrt{6} & \sqrt{2} \end{bmatrix} \begin{bmatrix} v_\alpha^* \\ v_\beta^* \end{bmatrix} \frac{T}{v_{dc}}$
	Triangle 3	$\begin{bmatrix} t_x \\ t_y \end{bmatrix} = \begin{bmatrix} -\sqrt{6} & \sqrt{2} \\ \sqrt{6} & \sqrt{2} \end{bmatrix} \begin{bmatrix} v_\alpha^* \\ v_\beta^* \end{bmatrix} \frac{T}{v_{dc}}$	Triangle 4	$\begin{bmatrix} t_x \\ t_y \end{bmatrix} = \begin{bmatrix} \sqrt{6} & \sqrt{2} \\ -\sqrt{6} & 0 \end{bmatrix} \begin{bmatrix} v_\alpha^* \\ v_\beta^* \end{bmatrix} \frac{T}{v_{dc}}$
Sector 3	Triangle 1	$\begin{bmatrix} t_x \\ t_y \end{bmatrix} = \begin{bmatrix} 0 & 2\sqrt{2} \\ -\sqrt{6} & \sqrt{2} \end{bmatrix} \begin{bmatrix} v_\alpha^* \\ v_\beta^* \end{bmatrix} \frac{T}{v_{dc}}$	Triangle 2	$\begin{bmatrix} t_x \\ t_y \end{bmatrix} = \begin{bmatrix} \sqrt{6}/2 & \frac{3}{2}\sqrt{2} \\ -\sqrt{6} & -\sqrt{2} \end{bmatrix} \begin{bmatrix} v_\alpha^* \\ v_\beta^* \end{bmatrix} \frac{T}{v_{dc}}$
	Triangle 3	$\begin{bmatrix} t_x \\ t_y \end{bmatrix} = \begin{bmatrix} -\sqrt{6} & -\sqrt{2} \\ 0 & 2\sqrt{2} \end{bmatrix} \begin{bmatrix} v_\alpha^* \\ v_\beta^* \end{bmatrix} \frac{T}{v_{dc}}$	Triangle 4	$\begin{bmatrix} t_x \\ t_y \end{bmatrix} = \begin{bmatrix} 0 & \sqrt{2} \\ -\sqrt{6}/2 & -\frac{3}{2}\sqrt{2} \end{bmatrix} \begin{bmatrix} v_\alpha^* \\ v_\beta^* \end{bmatrix} \frac{T}{v_{dc}}$
Sector 4	Triangle 1	$\begin{bmatrix} t_x \\ t_y \end{bmatrix} = \begin{bmatrix} -\sqrt{6} & \sqrt{2} \\ 0 & -2\sqrt{2} \end{bmatrix} \begin{bmatrix} v_\alpha^* \\ v_\beta^* \end{bmatrix} \frac{T}{v_{dc}}$	Triangle 2	$\begin{bmatrix} t_x \\ t_y \end{bmatrix} = \begin{bmatrix} -\sqrt{6}/2 & -\frac{3}{2}\sqrt{2} \\ 0 & -2\sqrt{2} \end{bmatrix} \begin{bmatrix} v_\alpha^* \\ v_\beta^* \end{bmatrix} \frac{T}{v_{dc}}$
	Triangle 3	$\begin{bmatrix} t_x \\ t_y \end{bmatrix} = \begin{bmatrix} 0 & -2\sqrt{2} \\ -\sqrt{6} & \sqrt{2} \end{bmatrix} \begin{bmatrix} v_\alpha^* \\ v_\beta^* \end{bmatrix} \frac{T}{v_{dc}}$	Triangle 4	$\begin{bmatrix} t_x \\ t_y \end{bmatrix} = \begin{bmatrix} -\sqrt{6} & \sqrt{2} \\ \sqrt{6}/2 & -\frac{3}{2}\sqrt{2} \end{bmatrix} \begin{bmatrix} v_\alpha^* \\ v_\beta^* \end{bmatrix} \frac{T}{v_{dc}}$

Sector 5	Triangle 1	$\begin{bmatrix} t_x \\ t_y \end{bmatrix} = \begin{bmatrix} -\sqrt{6} & -\sqrt{2} \\ \sqrt{6} & -\sqrt{2} \end{bmatrix} \begin{bmatrix} v_\alpha^* \\ v_\beta^* \end{bmatrix} \frac{T}{v_{dc}}$	Triangle 2	$\begin{bmatrix} t_x \\ t_y \end{bmatrix} = \begin{bmatrix} -\sqrt{6} & 0 \\ \sqrt{6} & -\sqrt{2} \end{bmatrix} \begin{bmatrix} v_\alpha^* \\ v_\beta^* \end{bmatrix} \frac{T}{v_{dc}}$
	Triangle 3	$\begin{bmatrix} t_x \\ t_y \end{bmatrix} = \begin{bmatrix} \sqrt{6} & -\sqrt{2} \\ -\sqrt{6} & -\sqrt{2} \end{bmatrix} \begin{bmatrix} v_\alpha^* \\ v_\beta^* \end{bmatrix} \frac{T}{v_{dc}}$	Triangle 4	$\begin{bmatrix} t_x \\ t_y \end{bmatrix} = \begin{bmatrix} -\sqrt{6} & -\sqrt{2} \\ \sqrt{6} & 0 \end{bmatrix} \begin{bmatrix} v_\alpha^* \\ v_\beta^* \end{bmatrix} \frac{T}{v_{dc}}$
Sector 6	Triangle 1	$\begin{bmatrix} t_x \\ t_y \end{bmatrix} = \begin{bmatrix} 0 & -2\sqrt{2} \\ \sqrt{6} & \sqrt{2} \end{bmatrix} \begin{bmatrix} v_\alpha^* \\ v_\beta^* \end{bmatrix} \frac{T}{v_{dc}}$	Triangle 2	$\begin{bmatrix} t_x \\ t_y \end{bmatrix} = \begin{bmatrix} -\sqrt{6}/2 & -\frac{3}{2}\sqrt{2} \\ \sqrt{6} & \sqrt{2} \end{bmatrix} \begin{bmatrix} v_\alpha^* \\ v_\beta^* \end{bmatrix} \frac{T}{v_{dc}}$
	Triangle 3	$\begin{bmatrix} t_x \\ t_y \end{bmatrix} = \begin{bmatrix} \sqrt{6} & \sqrt{2} \\ 0 & -2\sqrt{2} \end{bmatrix} \begin{bmatrix} v_\alpha^* \\ v_\beta^* \end{bmatrix} \frac{T}{v_{dc}}$	Triangle 4	$\begin{bmatrix} t_x \\ t_y \end{bmatrix} = \begin{bmatrix} 0 & -2\sqrt{2} \\ \sqrt{6}/2 & \frac{3}{2}\sqrt{2} \end{bmatrix} \begin{bmatrix} v_\alpha^* \\ v_\beta^* \end{bmatrix} \frac{T}{v_{dc}}$

Figure (A.1): Pulses generation of sector 2 to sector 6

Sector 2 :

T_s

	v_0	v_7	v_4	v_0	v_7	v_4	v_0	v_0	v_4	v_7	v_0	v_4	v_7	v_0
S_{2a}	0	0	1	1	1	1	1	1	1	1	1	1	0	0
S_{1a}	0	0	0	0	0	1	1	1	1	0	0	0	0	0
S_{2b}	0	1	1	1	1	1	1	1	1	1	1	1	1	0
S_{1b}	0	0	0	0	1	1	1	1	1	1	0	0	0	0
S_{2c}	0	0	0	1	1	1	1	1	1	1	1	0	0	0
S_{1c}	0	0	0	0	0	0	1	1	0	0	0	0	0	0
	$\frac{t_1}{6}$	$\frac{t_3}{4}$	$\frac{t_2}{4}$	$\frac{t_1}{6}$	$\frac{t_3}{4}$	$\frac{t_2}{4}$	$\frac{t_1}{6}$	$\frac{t_1}{6}$	$\frac{t_2}{4}$	$\frac{t_3}{4}$	$\frac{t_1}{6}$	$\frac{t_2}{4}$	$\frac{t_3}{4}$	$\frac{t_1}{6}$

(*triangle* 1 t_1, t_2, t_3)

T_s

	v_4	v_6	v_5	v_4	v_4	v_5	v_6	v_4
S_{2a}	1	1	1	1	1	1	1	1
S_{1a}	0	0	1	1	1	1	0	0
S_{2b}	1	1	1	1	1	1	1	1
S_{1b}	0	1	1	1	1	1	1	0
S_{2c}	0	0	0	1	1	0	0	0
S_{1c}	0	0	0	0	0	0	0	0
	$\frac{t_1}{4}$	$\frac{t_3}{2}$	$\frac{t_2}{2}$	$\frac{t_1}{4}$	$\frac{t_1}{4}$	$\frac{t_2}{2}$	$\frac{t_3}{2}$	$\frac{t_1}{4}$

(*triangle* 2 t_1, t_2, t_3)

T_s

	v_7	v_4	v_6	v_7	v_4	v_4	v_7	v_6	v_4	v_7
S_{2a}	0	1	1	1	1	1	1	1	1	0
S_{1a}	0	0	0	0	1	1	0	0	0	0
S_{2b}	1	1	1	1	1	1	1	1	1	1
S_{1b}	0	0	1	1	1	1	1	1	0	0
S_{2c}	0	0	0	1	1	1	1	0	0	0
S_{1c}	0	0	0	0	0	0	0	0	0	0
	$\frac{t_2}{4}$	$\frac{t_3}{4}$	$\frac{t_1}{2}$	$\frac{t_2}{4}$	$\frac{t_3}{4}$	$\frac{t_3}{4}$	$\frac{t_2}{4}$	$\frac{t_1}{2}$	$\frac{t_3}{4}$	$\frac{t_2}{4}$

(*triangle* 3 t_1, t_2, t_3)

T_s

	v_7	v_8	v_6	v_7	v_7	v_6	v_8	v_7
S_{2a}	0	0	1	1	1	1	0	0
S_{1a}	0	0	0	0	0	0	0	0
S_{2b}	1	1	1	1	1	1	1	1
S_{1b}	0	1	1	1	1	1	1	0
S_{2c}	0	0	0	1	1	0	0	0
S_{1c}	0	0	0	0	0	0	0	0
	$\frac{t_1}{4}$	$\frac{t_3}{2}$	$\frac{t_2}{2}$	$\frac{t_1}{4}$	$\frac{t_1}{4}$	$\frac{t_2}{2}$	$\frac{t_3}{2}$	$\frac{t_1}{4}$

$(triangle\ 4\ t_1, t_2, t_3)$

Sector 3 :

T_s

	v_0	v_7	v_{10}	v_0	v_7	v_4	v_0	v_0	v_{10}	v_7	v_0	v_{10}	v_7	v_0
S_{2a}	0	0	0	1	1	1	1	1	1	1	1	0	0	0
S_{1a}	0	0	0	0	0	0	1	1	0	0	0	0	0	0
S_{2b}	0	1	1	1	1	1	1	1	1	1	1	1	1	0
S_{1b}	0	0	0	0	0	1	1	1	1	0	0	0	0	0
S_{2c}	0	0	1	1	1	1	1	1	1	1	1	1	0	0
S_{1c}	0	0	0	0	0	1	1	1	1	0	0	0	0	0
	$\frac{t_1}{6}$	$\frac{t_2}{4}$	$\frac{t_3}{4}$	$\frac{t_1}{6}$	$\frac{t_2}{4}$	$\frac{t_3}{4}$	$\frac{t_1}{6}$	$\frac{t_1}{6}$	$\frac{t_3}{4}$	$\frac{t_2}{4}$	$\frac{t_1}{6}$	$\frac{t_3}{4}$	$\frac{t_2}{4}$	$\frac{t_1}{6}$

$(triangle\ 1\ t_1, t_2, t_3)$

T_s

	v_7	v_8	v_9	v_7	v_7	v_9	v_8	v_7
S_{2a}	0	0	0	1	1	0	0	0
S_{1a}	0	0	0	0	0	0	0	0
S_{2b}	1	1	1	1	1	1	1	1
S_{1b}	0	1	1	1	1	1	1	0
S_{2c}	0	0	1	1	1	1	0	0
S_{1c}	0	0	0	0	0	0	0	0
	$\frac{t_1}{4}$	$\frac{t_2}{2}$	$\frac{t_3}{2}$	$\frac{t_1}{4}$	$\frac{t_1}{4}$	$\frac{t_3}{2}$	$\frac{t_2}{2}$	$\frac{t_1}{4}$

(*triangle* 2 t_1, t_2, t_3)

T_s

	v_7	v_{10}	v_9	v_7	v_{10}	v_{10}	v_7	v_9	v_{10}	v_7
S_{2a}	0	0	0	1	1	1	1	0	0	0
S_{1a}	0	0	0	0	0	0	0	0	0	0
S_{2b}	1	1	1	1	1	1	1	1	1	1
S_{1b}	0	0	1	1	1	1	1	1	0	0
S_{2c}	0	1	1	1	1	1	1	1	1	0
S_{1c}	0	0	0	0	1	1	0	0	0	0
	$\frac{t_3}{4}$	$\frac{t_2}{4}$	$\frac{t_1}{2}$	$\frac{t_3}{4}$	$\frac{t_2}{4}$	$\frac{t_2}{4}$	$\frac{t_3}{4}$	$\frac{t_1}{2}$	$\frac{t_2}{4}$	$\frac{t_3}{4}$

(*triangle* 3 t_1, t_2, t_3)

T_s

	v_{10}	v_9	v_{11}	v_{10}	v_{10}	v_{11}	v_9	v_{10}
S_{2a}	0	0	0	1	1	0	0	0
S_{1a}	0	0	0	0	0	0	0	0
S_{2b}	1	1	1	1	1	1	1	1
S_{1b}	0	1	1	1	1	1	1	0
S_{2c}	1	1	1	1	1	1	1	1
S_{1c}	0	0	1	1	1	1	0	0
	$\frac{t_1}{4}$	$\frac{t_3}{2}$	$\frac{t_2}{2}$	$\frac{t_1}{4}$	$\frac{t_1}{4}$	$\frac{t_2}{2}$	$\frac{t_3}{2}$	$\frac{t_1}{4}$

$(triangle\ 4\ \mathrm{t}_1, t_2, t_3)$

Sector 4 :

T_s

	v_0	v_{13}	v_{10}	v_0	v_{13}	v_{10}	v_0	v_0	v_{10}	v_{13}	v_0	v_{10}	v_{13}	v_0
S_{2a}	0	0	0	1	1	1	1	1	1	1	1	0	0	0
S_{1a}	0	0	0	0	0	0	1	1	0	0	0	0	0	0
S_{2b}	0	0	1	1	1	1	1	1	1	1	1	1	0	0
S_{1b}	0	0	0	0	0	1	1	1	1	0	0	0	0	0
S_{2c}	0	1	1	1	1	1	1	1	1	1	1	1	1	0
S_{1c}	0	0	0	0	1	1	1	1	1	1	0	0	0	0
	$\frac{t_1}{6}$	$\frac{t_3}{4}$	$\frac{t_2}{4}$	$\frac{t_1}{6}$	$\frac{t_3}{4}$	$\frac{t_2}{4}$	$\frac{t_1}{6}$	$\frac{t_1}{6}$	$\frac{t_2}{4}$	$\frac{t_3}{4}$	$\frac{t_1}{6}$	$\frac{t_2}{4}$	$\frac{t_3}{4}$	$\frac{t_1}{6}$

$(triangle\ 1\ \mathrm{t}_1, t_2, t_3)$

T_s

	v_{10}	v_{12}	v_{11}	v_{10}	v_{10}	v_{11}	v_{12}	v_{10}
S_{2a}	0	0	0	1	1	0	0	0
S_{1a}	0	0	0	0	0	0	0	0
S_{2b}	1	1	1	1	1	1	1	1
S_{1b}	0	0	1	1	1	1	0	0
S_{2c}	1	1	1	1	1	1	1	1
S_{1c}	0	1	1	1	1	1	1	0
	$\frac{t_1}{4}$	$\frac{t_3}{2}$	$\frac{t_2}{2}$	$\frac{t_1}{4}$	$\frac{t_1}{4}$	$\frac{t_2}{2}$	$\frac{t_3}{2}$	$\frac{t_1}{4}$

(*triangle* 2 t_1, t_2, t_3)

T_s

	v_{13}	v_{10}	v_{12}	v_{13}	v_{10}	v_{10}	v_{13}	v_{12}	v_{10}	v_{13}
S_{2a}	0	0	0	1	1	1	1	0	0	0
S_{1a}	0	0	0	0	0	0	0	0	0	0
S_{2b}	0	1	1	1	1	1	1	1	1	0
S_{1b}	0	0	0	0	1	1	0	0	0	0
S_{2c}	1	1	1	1	1	1	1	1	1	1
S_{1c}	0	0	1	1	1	1	1	1	0	0
	$\frac{t_2}{4}$	$\frac{t_3}{4}$	$\frac{t_1}{2}$	$\frac{t_2}{4}$	$\frac{t_3}{4}$	$\frac{t_3}{4}$	$\frac{t_2}{4}$	$\frac{t_1}{2}$	$\frac{t_3}{4}$	$\frac{t_2}{4}$

(*triangle* 3 t_1, t_2, t_3)

T_s

	v_{13}	v_{14}	v_{12}	v_{13}	v_{13}	v_{12}	v_{14}	v_{13}
S_{2a}	0	0	0	1	1	0	0	0
S_{1a}	0	0	0	0	0	0	0	0
$S_{2б}$	0	0	1	1	1	1	0	0
$S_{1б}$	0	0	0	0	0	0	0	0
S_{2c}	1	1	1	1	1	1	1	1
S_{1c}	0	1	1	1	1	1	1	0
	$\frac{t_1}{4}$	$\frac{t_3}{2}$	$\frac{t_2}{2}$	$\frac{t_1}{4}$	$\frac{t_1}{4}$	$\frac{t_2}{2}$	$\frac{t_3}{2}$	$\frac{t_1}{4}$

(*triangle* 4 t_1, t_2, t_3)

Sector 5 :

T_s

	v_0	v_{13}	v_{16}	v_0	v_{13}	v_{16}	v_0	v_0	v_{16}	v_{13}	v_0	v_{16}	v_{13}	v_0
S_{2a}	0	0	1	1	1	1	1	1	1	1	1	1	0	0
S_{1a}	0	0	0	0	0	1	1	1	1	0	0	0	0	0
$S_{2б}$	0	0	0	1	1	1	1	1	1	1	1	0	0	0
$S_{1б}$	0	0	0	0	0	0	1	1	0	0	0	0	0	0
S_{2c}	0	1	1	1	1	1	1	1	1	1	1	1	1	0
S_{1c}	0	0	0	0	1	1	1	1	1	1	0	0	0	0
	$\frac{t_1}{6}$	$\frac{t_2}{4}$	$\frac{t_3}{4}$	$\frac{t_1}{6}$	$\frac{t_2}{4}$	$\frac{t_3}{4}$	$\frac{t_1}{6}$	$\frac{t_1}{6}$	$\frac{t_3}{4}$	$\frac{t_2}{4}$	$\frac{t_1}{6}$	$\frac{t_3}{4}$	$\frac{t_2}{4}$	$\frac{t_1}{6}$

(*triangle* 1 t_1, t_2, t_3)

T_s

	v_{10}	v_{12}	v_{11}	v_{10}	v_{10}	v_{11}	v_{12}	v_{10}
S_{2a}	0	0	0	1	1	0	0	0
S_{1a}	0	0	0	0	0	0	0	0
S_{2b}	1	1	1	1	1	1	1	1
S_{1b}	0	0	1	1	1	1	0	0
S_{2c}	1	1	1	1	1	1	1	1
S_{1c}	0	1	1	1	1	1	1	0
	$\frac{t_1}{4}$	$\frac{t_3}{2}$	$\frac{t_2}{2}$	$\frac{t_1}{4}$	$\frac{t_1}{4}$	$\frac{t_2}{2}$	$\frac{t_3}{2}$	$\frac{t_1}{4}$

(*triangle* 2 t_1, t_2, t_3)

T_s

	v_{13}	v_{16}	v_{15}	v_{13}	v_{16}	v_{16}	v_{13}	v_{15}	v_{16}	v_{13}
S_{2a}	0	1	1	1	1	1	1	1	1	0
S_{1a}	0	0	0	0	1	1	0	0	0	0
S_{2b}	0	0	0	1	1	1	1	0	0	0
S_{1b}	0	0	0	0	0	0	0	0	0	0
S_{2c}	1	1	1	1	1	1	1	1	1	1
S_{1c}	0	0	1	1	1	1	1	1	0	0
	$\frac{t_3}{4}$	$\frac{t_2}{4}$	$\frac{t_1}{2}$	$\frac{t_3}{4}$	$\frac{t_2}{4}$	$\frac{t_2}{4}$	$\frac{t_3}{4}$	$\frac{t_1}{2}$	$\frac{t_2}{4}$	$\frac{t_3}{4}$

(*triangle* 3 t_1, t_2, t_3)

T_s

	v_{16}	v_{15}	v_{17}	v_{16}	v_{16}	v_{17}	v_{15}	v_{16}
S_{2a}	1	1	1	1	1	1	1	1
S_{1a}	0	0	1	1	1	1	0	0
S_{2b}	0	0	0	1	1	0	0	0
S_{1b}	0	0	0	0	0	0	0	0
S_{2c}	1	1	1	1	1	1	1	1
S_{1c}	0	1	1	1	1	1	1	0
	$\frac{t_1}{4}$	$\frac{t_2}{2}$	$\frac{t_3}{2}$	$\frac{t_1}{4}$	$\frac{t_1}{4}$	$\frac{t_3}{2}$	$\frac{t_2}{2}$	$\frac{t_1}{4}$

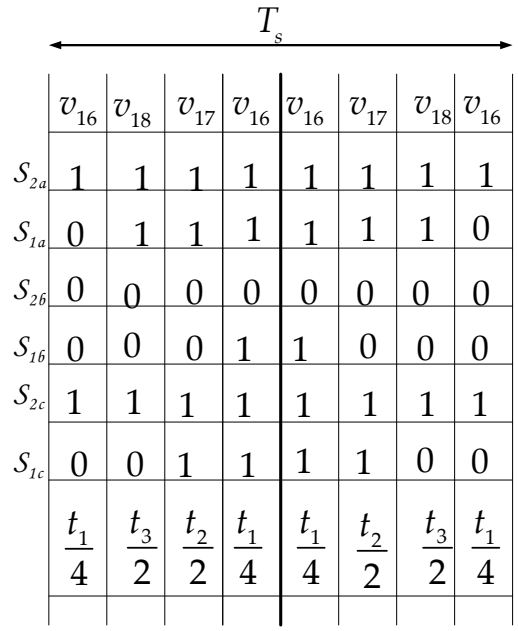
(*triangle* 4 t_1, t_2, t_3)

Sector 6 :

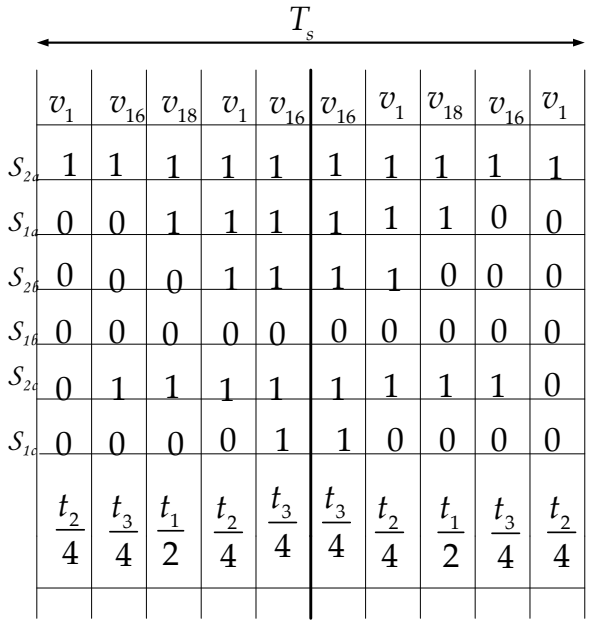
T_s

	v_0	v_1	v_{16}	v_0	v_1	v_{16}	v_0	v_0	v_{16}	v_1	v_0	v_{16}	v_1	v_0
S_{2a}	0	1	1	1	1	1	1	1	1	1	1	1	1	0
S_{1a}	0	0	0	0	1	1	1	1	1	0	0	0	0	0
S_{2b}	0	0	0	1	1	1	1	1	1	1	1	0	0	0
S_{1b}	0	0	0	0	0	0	1	1	0	0	0	0	0	0
S_{2c}	0	0	1	1	1	1	1	1	1	1	1	1	0	0
S_{1c}	0	0	0	0	0	1	1	1	1	0	0	0	0	0
	$\frac{t_1}{6}$	$\frac{t_3}{4}$	$\frac{t_2}{4}$	$\frac{t_1}{6}$	$\frac{t_3}{4}$	$\frac{t_2}{4}$	$\frac{t_1}{6}$	$\frac{t_1}{6}$	$\frac{t_2}{4}$	$\frac{t_3}{4}$	$\frac{t_1}{6}$	$\frac{t_2}{4}$	$\frac{t_3}{4}$	$\frac{t_1}{6}$

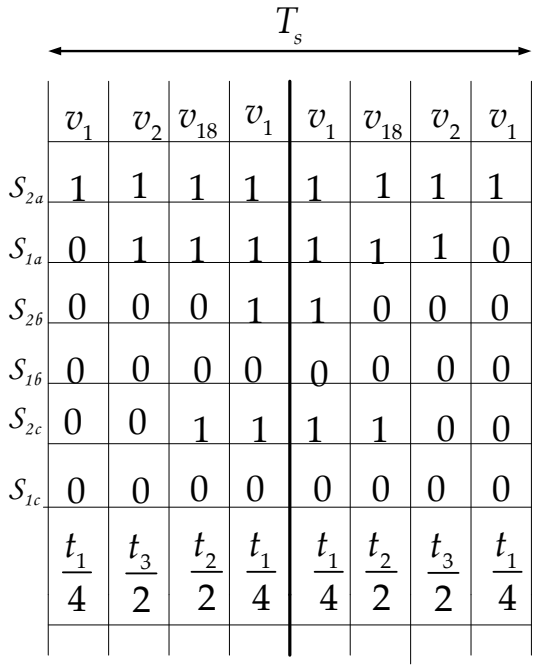
(*triangle* 1 t_1, t_2, t_3)



(*triangle* 2 t_1, t_2, t_3)



(*triangle* 3 t_1, t_2, t_3)



(*triangle* 4 t_1, t_2, t_3)

Basic Definitions

1- Harmonic Distortion (HD)

$$HD = \frac{X_n}{X_1} \times 100\%$$

X_1 : RMS value of first harmonic of voltage or current

X_n : RMS value of n harmonic of voltage or current

2- Total Harmonic Distortion (THD)

$$THD = \frac{\sqrt{\sum_{n>1} X_n^2}}{X_1} \times 100\%$$

X_1 : RMS value of first harmonic of voltage or current

X_n : RMS value of n harmonic of voltage or current

Abstract

In comparison with conventional two-level inverters, multilevel inverters present lower switching losses, lower voltage stress on switching devices, lower common-mode voltages and better harmonic performance. Due to these remarkable features, nowadays the application of this technology covers a wide range, where high-quality voltages and currents are required. This thesis presents an FPGA based implementation of space vector modulation for three-level diode clamped inverter. The three-level inverter using SVM control has superior performance though bringing about much computational complexity. Therefore, the XILINX Zynq 7000 FPGA-based implementation could solve this problem well.

Keywords

Multilevel converters, Three-level diode clamped inverter, Space vector modulation, FPGA.

ملخص

بالمقارنة مع المحولات التقليدية ذات مستويين، فإن المحولات متعددة المستويات تقدم خسائر أقل في التحويل، توتر كهربائي أقل على أجهزة التحويل ، جهد فولتي مشترك أقل وأداء توافقي أفضل. نظرًا لهذه الميزات الرائعة ، فإن تطبيق هذه التكنولوجيا يغطي في الوقت الحاضر نطاقًا واسعًا، حيث تكون الجودة العالية للتيارات الكهربائية و التوترات مطلوبة. تقدم هذه المذكرة تنفيذ يعتمد على FPGA للتعديل الشعاعي لعرض النبضة من أجل المحول ذي ثلاث مستويات. يتميز المحول ذو الثلاث مستويات الذي يستخدم تحكم التعديل الشعاعي لعرض النبضة بأداء فائق مع تحقيق الكثير من التعقيد الحسابي . لذلك، يمكن تطبيق -XILINX Zynq 7000 FPGA إلى حل هذه المشكلة بشكل جيد.

كلمات مفتاحية:

محول متعدد المستويات، العاكس ذي ثلاث مستويات مع الصمامات الثنائية العائمة، التعديل الشعاعي لعرض النبضة، FPGA.