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Thème :

Multi objective Optimal Allocation of Superconducting Fault Current Limiters (SFCLs) in Electrical Power System

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ملخص:

في هذا العمل ، تم تقديم خوارزمية التحسين المستندة إلى باريتو ، وهي خوارزمية MOPSO Multiobjective Particle Optimization Optimization لتحديد العدد والموقع الأمثل لمحدِّدات تيار عطل LCD لتقليل تأثير تيار الدائرة القصيرة في الشبكة الكهربائية وفقًا لهدف مختلف المهام. تم اختيار الشبكة الكهربائية IEEE 30 BUS لتقييم كفاءة وجدوى التقنية المقترحة. تتمثل الوظائف الموضوعية التي تم النظر فيها للتخصيص الأمثل في تقليل تيار الدائرة القصيرة في النظام الكهربائي والأثر الاقتصادي (عدد ومقاومة شاشات LCD). جعل استخدام هذه الطريقة من الممكن الحصول على أفضل جبهة باريتو التي يتم فيها تحسين هذه الوظائف الموضوعية في وقت واحد.

Abstract:

In this work, Pareto based optimization algorithm, namely multiobjective particle swarm optimization a MOPSO algorithm, is presented to determine the optimal number and location of FCLs to reduce the short circuit current effect in the power network based on different conflicting objective functions. IEEE 30 BUS system is considered to evaluate the effectiveness and feasibility of the proposed technique. The objective functions considered for the optimal allocation are short circuit current reduction in power system, and economic impact. The use of this method made it possible to obtain the Pareto optimal front in which these objective functions are optimized simultaneously.

Résumé :

Dans ce travail, un algorithme d'optimisation basé sur Pareto, à savoir l'algorithme d'optimisation d'un essaim de particules multiobjective MOPSO est présenté pour déterminer le nombre et l'emplacement optimaux des limiteurs de courant de défauts LCD afin de réduire l'effet de courant de court-circuit dans le réseau électrique en fonction de différentes fonctions objectives. Le réseau électrique IEEE 30 BUS est choisi pour évaluer l'efficacité et la faisabilité de la technique proposée. Les fonctions objectives considérées pour l'allocation optimale sont la réduction du courant de court-circuit dans le système électrique et l'impact économique (nombre et l'impédance de LCD). L'utilisation de cette méthode a permis d'obtenir le front optimal de Pareto dans lequel ces fonctions objectives sont optimisées simultanément.

Summary

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Chapter III

List of symbols and abbreviations

Symbol	Explanation
SFCL	**Supraconducting Fault Current Limiter**
DG	Distributed Generation
L V	Low voltage
H V	High voltage
Pu	Pre-unit
FCL	Fault current limiter
MOPSO	Multiple Objective Particle Swarm Optimization
S C	Superconductor
Z Bus	Impedance matrix of network
HTS	High Temperature Superconductor
SSFCL	Solid-state Fault Current Limiter
$\mathbf{Z_L}$	Impedance of line
$\mathbf{Z_{FCL}}$	Impedance of FCL
$\mathbf{N_{SFCL}}$	Number of SFCLs
$\mathbf{I^{SC\ MAX}}$	Rating current of CB
F	Objective function value

General Introduction

Introduction

With the increasing electric power demand, power systems has become bigger and more complex, and as a result, fault current have risen. In some cases, raising the fault current can lead the acceptable level of network equipment, particularly circuit breakers (CBs), to exceed the allowable level and even damage certain types of equipment. As a result, CBs with a larger breaking current are required. As a result, the operating system significant costs. If, after identifying the fault, the current, can be clearly limited by a method, technically and economically significant that carried out by Fault current limiters (FCLs) [1].

FCLs are elements placed in parallel with network equipment to reduce tripping current running during a fault normally; this equipment showed low resistance to the fault current. However, if a short circuit occurs and their resistance suddenly increases in the initial moments after the fault, more short circuit current is avoided [2]. Limiters do not cause voltage sag or power loss in the system's steady state conditions [3].

Literature review

The transient stability due to the use of FCLs in the network has been investigated in reference [4], by studying the generator's rotor oscillation after the occurrence of a big amplitude fault, e.g. short circuit. [5] discusses the use of a superconducting fault current limiter (SFCL) to improve the power system transient stability. In Ref. [6,] the enhancement of power system security and stability is investigated, and the particle swarm optimization (PSO) technique is employed to optimize the system. [7] addresses two aspects of FCL use in the distribution network: fault current limitation and voltage sag suppression. FCLs' effect on the distribution network in Wind turbine generators are being investigated [8].

This work focuses on the fault current limiting impact of FCLs. In addition to short circuit current limitations, studies have shown that the use of FCLs in power networks enhances generator transient stability and, as a consequence, network global stability [9, 10]. Previous research on FCL optimal allocation have mostly focused on one objective function, such as fault reduction [11–13] or stability [9,13].

The effectiveness of FCL depends on the number of FCLs and their installation location. In this work, a metaheuristic technique is applied to determine the optimal number and location of FCLs to reduce fault current in the IEEE 30-bus system. The objective functions considered for the optimal allocation are short circuit current reduction, impedance size, number and location of FCLs. A Pareto based multiobjective particle swarm optimization (MOPSO), is utilized to deal with this problem. The use of this

approach made it possible to obtain the Pareto optimal front in which these objective functions, are optimized simultaneously.

This thesis is structured as follows:

Superconducting fault current limiters SFCL is discussed in chapter 1. It begins with model of a SFCL and a brief introduction to the application of current limiting Technologies.

Chapter 2 present the impact of SFCLs in electrical power system.

The simulation results and discussion are display in chapter 3.

We finished this work with general conclusion.

Chapter I

Superconducting fault current limiters

Introduction

Superconductors are unique materials that allow for the passage of electrical energy with little losses, making them extremely promising for electrical engineering applications. This chapter opens with a brief history and definition of superconductors, as well as their essential features. The various types of superconductors (type I and type II) will next be discussed. Then there are several superconductor models. Finally, we will discuss the most common uses of superconductors in electrical engineering, as well as existing constraints in electrical networks

Model of a superconducting fault current limiter SFCL

The SFCL can be represented by impedance, which changes with current and/or temperature or resistance, which changes with time. The second representation is more straightforward.

The second method is faster than the first and allows for shorter simulation duration. Because the time required to recover a stability point in an EPG in the event of a breakdown is many seconds, a precise SFCL model is not required in our situation. The resistance of the SFCL employed in the simulation may be described as follows:

Where RSFCL and are the maximum resistance that the SFCL may impose in the transmission line and the time it takes for the superconducting state to shift to the normal state because the amount of the fault current in high voltage (HV) lines is less relevant than in low voltage (LV) lines, the SFCL model has been adopted in simulations (the ratio between these two line currents is defined by the ratio of the primary and secondary voltages of transformers). In reality, the SFCL units needed to restrict the fault current in HV will be less critical than in LV As a result, it would be simpler to implement the SFCL design in HV.

We live in a world interested in power. Everything around us requires power, from small appliances in private homes to large-scale motors in factories, leading in an ever-increasing demand for electrical energy. Consequently, there is always a need for expanded generation capacity to satisfy energy requirements. Nevertheless, in power systems, increasing generation capacity and decreasing fault current levels frequently go hand in hand. As a result, a rise in energy demand necessitates an increase in generating capacity, while a drop in fault current level is required to maintain the system safe and stable. Fault current limiters, as the name implies, are used to lower the amount of fault currents and therefore the compromise on power system stability in the event of a fault. It is based on producing a wide

series resistance in the path of fault currents in the event of a fault, whereas resistance in the path of current is negligible in normal situations.

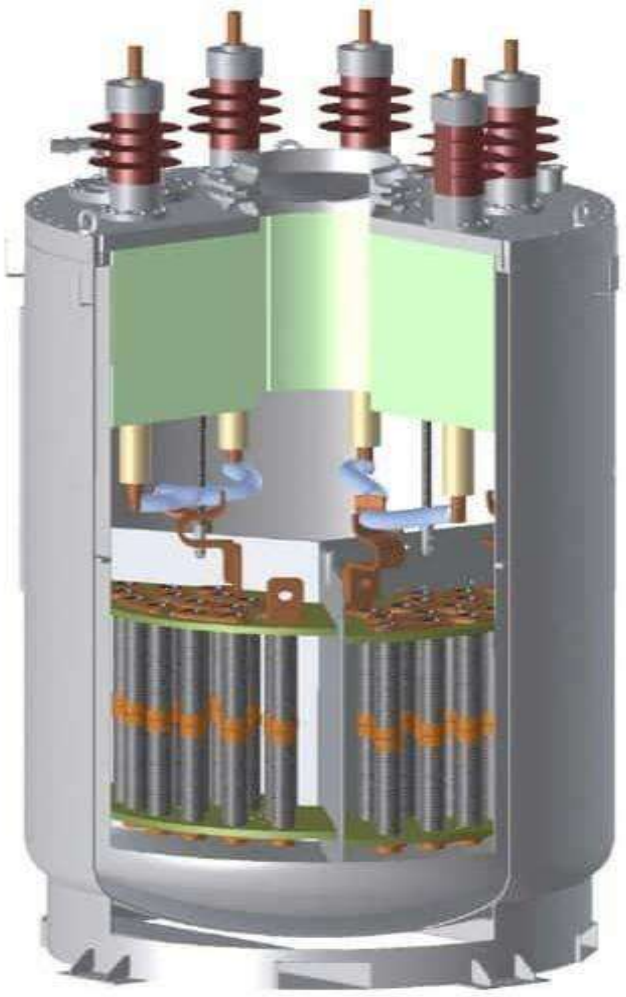

Figure I.1: Transformer-like saturated core Fault current limiter.

Application of Current Limiting Technologies

When a short circuit occurs in a power network, the fault current rapidly increases. The pace at which the current rises is determined by the source voltage, source impedance, and fault phase angle. Figure 1.1 depicts a typical potential short circuit current waveform compared to currents under current limiting methods. It denotes the three fundamental operational regimes [1, 2]:

- Normal operation in which no defect occurs and no restricting steps are taken;
- Fault condition: limitless or limited;
- Recovery interval during which the system returns to normal operation.

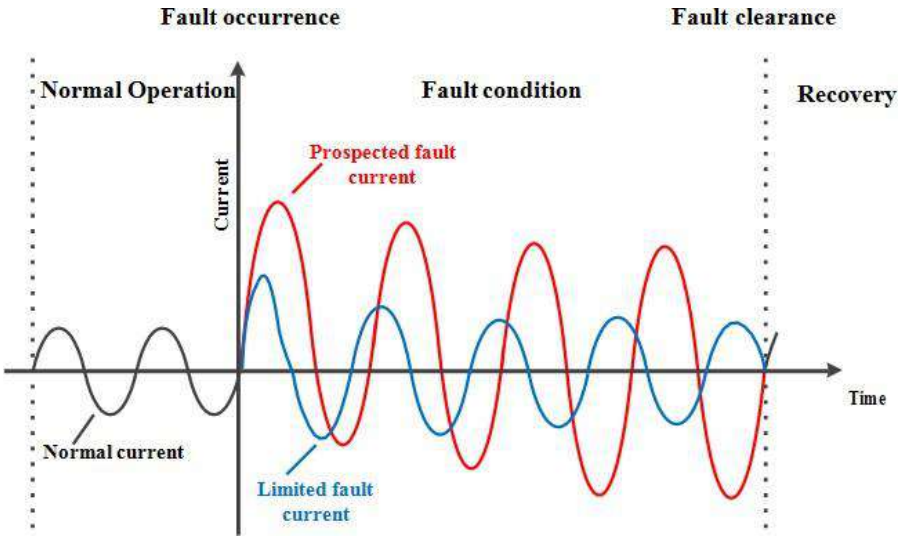

Figure I.2: Typical fault current waveforms with and without fault current limiting technologies.

Given the dangers of excessive fault currents to both power system equipment and workers, appropriate methods to lower fault current levels must be implemented. Conventional solutions for minimizing fault current may be divided into three broad categories:

• Permanent impedance increase: in this case, the system impedance will be increased under both normal and fault conditions, including topological measures such as sub-grid splitting and bus-bar splitting to reduce interconnections; [14, 15]or increasing system voltage levels because the system impedance could be increased when the power base remains unchanged; and apparatus measures such as installing high impedance transformers and current limiting reactors..

• Condition-based impedance increase: this technique only adds impedance to the network when there is a failure, such as by introducing fuse-based devices, stand-alone HV fuses, fuse-based limiters, or novel concept fault current limiters.

• Control strategy, such as sequential CB tripping.

Considering the danger of high fault currents to both power system equipment and working personnel, appropriate measures to lower fault current levels must be implemented. There are three basic types of conventional strategies for limiting fault current:

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splitting and bus-bar splitting to reduce interconnections, or increasing system voltage levels so because system impedance may be increased when the power base remains unchanged; and apparatus measures such as installing high impedance transformers and current limiting reactors.

• Condition-based impedance increase: this method only contributes impedance to the network when there is a problem, such as when introducing fuse-based devices, stand-alone HV fuses, fuse-based limiters, or innovative concept fault current limiters.

• Control strategy, such as sequential CB tripping.

Increase source impedance

The simplest way to reduce the fault is to increase the source impedance. This could be achieved by installing [16] devices such as air-cooled reactors or transformers with relatively high reactance. However, this results in additional voltage drop, reactive power, and a potentially high transient recovery voltage (TRV).

Reduce network interconnection

Changing the network topology, which typically involves splitting bus bars by opening a bus bar section or bus coupler, is one method for reducing the fault current level. As a corollary, the grid can be divided [17] into smaller parts that can be supplied by a lower voltage level. However, since this technique separates sources from loads, the supply's security is weakened. Meanwhile, this method may result in increased losses, reduced voltages, and decreased grid flexibility [18].

Increase system voltage

By raising the voltage levels, the fault current can be minimized. For example, with certain power delivery, increasing the voltage level from 11 kV to 22 kV allows system impedance to grow four times while reducing the fault current by half. However, this method is impractical in practice due to the higher expenses of high voltage equipment in substations.

Sequential CB tripping

A protection scheme that is occasionally used is sequential tripping of CBs, which generally involves opening an upstream CB [19] (normally remote from the fault) that is rated to switch the maximum prospective fault current. The downstream CB (the one nearest to the fault) can then be opened, which has a much lower rating and a lower price. The upstream CB is again re-closed [20].

Since it alters the system topology during the fault, this measure can be considered a fault current limiting method since it reduces the fault current duty of the interrupting device. However, the disadvantages of this method are apparent. To start with, the total time necessary to remove the issue and restore the load will be increased. Second, creating an upstream CB disrupts a much larger zone of the electrical system than opening a downstream CB.

Fault current limiter

Fault Current Limiters (FCLs) are devices which detect, trigger, and limit dangerous fault currents in electrical power systems. Under normal operating conditions, an ideal FCL has near-zero impedance, leading in minimal voltage drop and, more importantly, no extra power losses. In contrast, during fault conditions, the FCL could quickly detect the instantaneously increased fault current. The FCL would then be changed to a high impedance state, decreasing the fault current. Furthermore, if the fault is cleared, it might revert to a low impedance state [21].

Types of Fault Current Limiters

The most commonly used types of FCLs are:

- Superconductive FCLs
- Non-superconductive FCLs

Super Conductive FCLs (SFCLs)

Type superconductive FCLs work on the superconductivity principle. During normal conditions, it acts as a superconductor to virtually no resistance in the path, but during a fault, its critical temperature is managed [22]to reach due to an increase in temperature caused by a highfault current, and it changes its state from superconducting to normal to high resistance, restricting fault current.[23]

There really are two types of SFCL.

Resistive Type SFCL

During normal operation, resistive type SFCL uses superconducting material as a conductor to carry current. The current flows via the superconducting element Rsc during normal operation. During normal operation, the heat generated by normal current maintains the SFCL below its critical temperature, but during a fault, the temperature rises above the critical temperature of the superconductor utilized.[24] When the current reaches the

maximum,

the temperature goes up, forcing the superconductor to transform from superconductor to resistor, adding more resistance than normal in the fault current's path, and limiting the fault current. This phenomenon is known as "quenching." When the defect is removed, the substance returns to its superconducting condition. The temperature falls below the critical temperature of the superconductor. To avoid over-voltages produced by fast current limitations during the quench, inductive shunt ZSH or parallel resistance is used.[25]

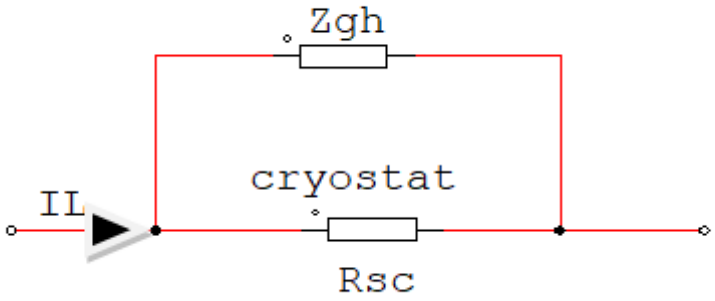

Figure I.3: Resistive Type Superconducting Fault Current Limiter.

Inductive Type SFCL

This type of SFCL does have a construction similar to transformers with a secondary winding made of a superconducting element. During normal operation, the resistance of the primary winding and the leakage reactance determine the impedance of the limiter since the resistance of the secondary is practically zero so because superconductor's temperature is kept below the critical temperature. The resistance of the secondary winding increases during fault conditions, and the superconductor quenches the fault by transforming itself into a resistor. The secondary value (RSC) is transferred to the primary side, increasing the effective impedance of the line. This type of SFCL is larger and heavier than resistive SFCL.[26]

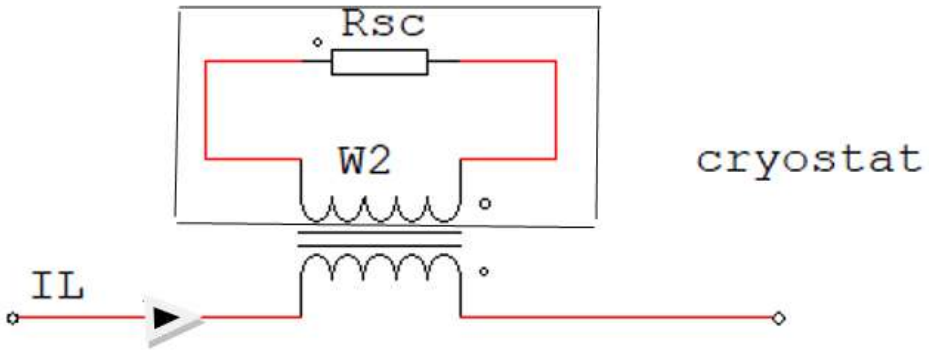

Figure I.4: Inductive Type Superconducting Fault Current limiter.

Non-Super Conductive FCLs

These FCLs do not use superconducting elements and are built in such a way that resistance is bypassed during normal operation but a substantial resistance is realized to limit currents in defective situations. The major types of non-superconductive FCLs are as following.

Saturated Core FCLs

They achieve the highest inductance by taking use of the nonlinear properties of ferromagnetic materials. Usually, the core of ferromagnetic material is biased by DC current to make it saturated, and as a function, has rather little inductance in line. The core becomes unsaturated [27] during faults, resulting in a high inductance in the current path to limit current flow.

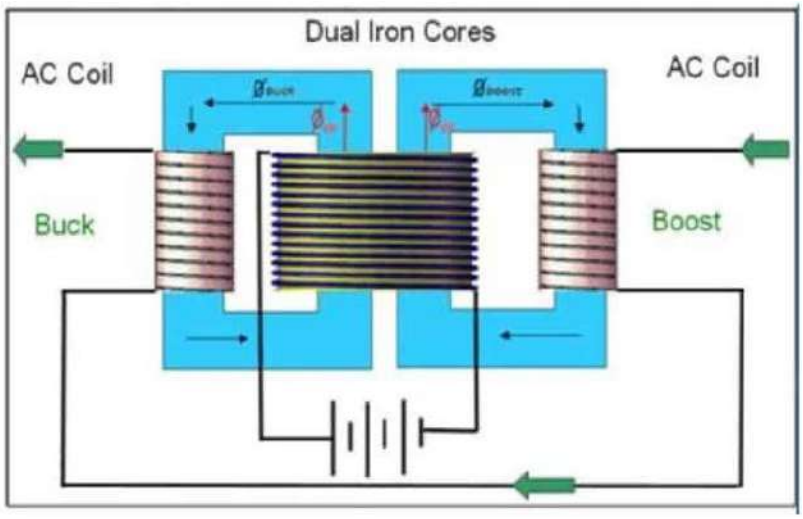

Figure I.5: Saturated core Fault Current Limiters.

Solid-state FCLs (SFCLs)

In normal conditions, these FCLs use electronic switching to bypass resistances and introduce resistance in abnormal conditions. Bi-directional controlled switches on serial SSFCLs bypass either the normal or faulty state.[28]

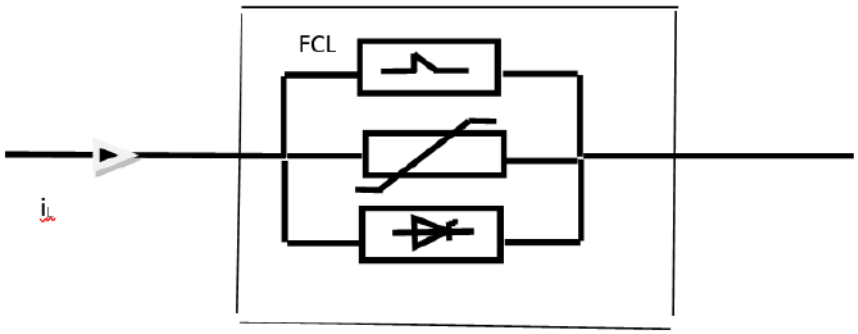

Figure I.6: Serial type Solid-state Fault Current Limiters

Bridge type SSFCL uses Thyristor to make a bridge arrangement. Switching is done in such a manner that when there is a defect, resistance is also included in the circuit and current decreases.

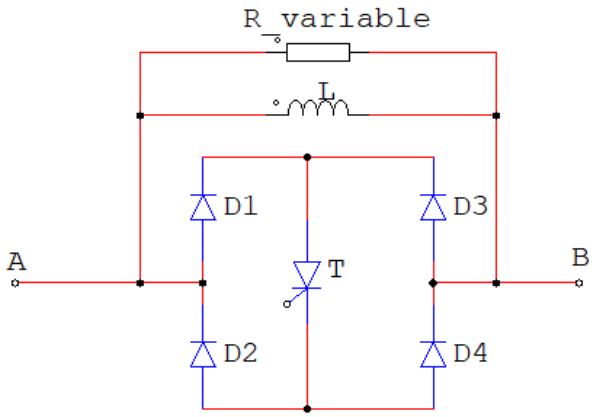

Figure I.7: Bridge type Solid-state Fault Current Limiters.

The phenomenon of resonance is used in the resonance type SSSFCL. Since we know that the resistance of a circuit is greatest during resonance, a series resonance circuit is being used to match the line frequency under normal conditions. During a defect, the topology of the circuit changes, and the circuit no longer remains in resonance, offering much higher impedance inline impedance inline.[29]

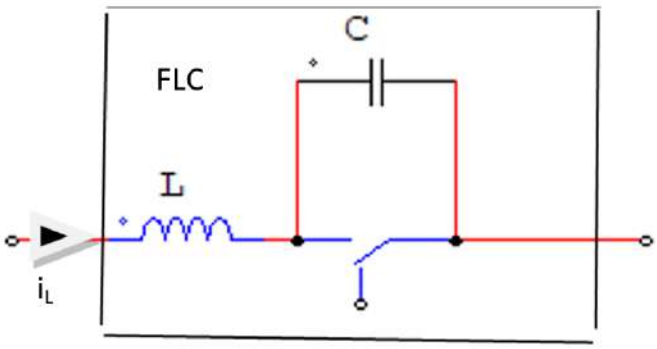

Figure I.8: Resonance type Solid-state Fault Current Limiters.

Advantages of Fault Current Limiters

- It limits the current to prevent damage to equipment
- It prevents the replacement of costly component
- It enhances the stability of power systems

Conclusion

A brief description of fault current limiters (FCLs) reduce fault currents without compromising circuit characteristics, is given in this chapter. It keeps equipment from being damaged and enhances system stability. Although FCL has many advantages, one of the main disadvantages is the introduction of resistance and power losses, which are negligible in normal conditions.

Chapter 2 present the impact of SFCLs in electrical power system.

Chapter II

Impact of SFCLs in Electrical Power System

II.1Introduction

This chapter focuses on the fault current limiting impact of FCLs. In addition to short circuit current limitations, studies have shown that the use of FCLs in power networks enhances generator transient stability and, as a consequence, network global stability [1,2]. Previous research on FCL optimal allocation have mostly focused on one objective function, such as fault reduction [3–4] or stability [1,4].

II.2 Fault current calculation and the effect of adding a FCLonZ_{BUS} impedance

Because it is the worst type of fault, three phases of symmetrical faults are used to specify the CBS rating. The short-circuit current for a balanced three-phase fault over bus I can be calculated as follows:

$$I_I^{SC} = \frac{EI}{Zii} * Ib \qquad \text{(II.1)}$$

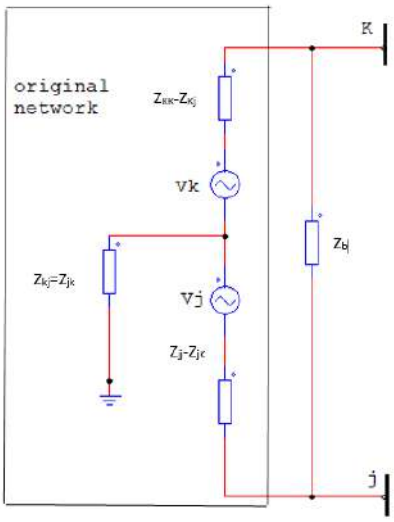

Figure II.1: Thevenin equivalent when line is added between *k* and *j* buses

where *Isc* is the three-phase short circuit current at the bus *i* and *Ei* is the voltage before the fault at bus *i*. Commonly, *I* can be set as 1 p.u. The parameter Z_{ii} is the diagonal impedance of the impedance matrix (Z_{bus}) and I_b is the base current [12]. When adding a line with impedance Z_b between buses *j* and *k*, each element of Z_{bus} can be modified as follows:

$$Z_{XY}^{NEW} = Z_{xy}^{old} - \frac{(Zxj - Zxk)(Zjy - Zky)}{zjj + zkk - 2Zjk + Zb} \qquad \text{(II.2)}$$

Where Z_{new} and Z_{old} are the modified and old Z_{bus} elements, respectively. Moreover, the impact of inserting the impedance Z_b series with the transmission line can

be viewed as a parallel impedance Zp with the network, as seen below.

$$Z_p = (Z_B)//(Z_B + Z_{FCL}) = -\frac{Zb(Zb+Zfcl)}{ZFCL} \quad \text{(II.3)}$$

By viewing the system from two existing buses to impedance Zb put between them, the Thevenin equivalent is represented. The following adjustments were introduced to the diagonal entries of Zbus after the FCL is triggered at a branch between buses j and k:

$$\Delta Zii = -\frac{(Zjj-Zik)^2}{Zjj+Zkk-2Zjk+Zp} \quad \text{(II.4)}$$

Problemformulation

The optimal allocation of FCL is a nonlinear optimization problem with several objective functions. The objective functions considered in this study are reliability enhancement, economical the use FCLs, and short circuit current reduction. The above are the objective functions:

Fault current calculation and fault current limiters

The majority of faults in power systems are symmetrical; however, the three-phase fault is the most severe which is used to specify circuit breaker values. The following sections detail the calculation of fault current at each bus and the effect of three-phase faults on the currents flowing in the lines:

Fault current calculation

For asymmetrical fault at busit he fault current can be obtained by(1):

$$f(x) = I_i^{sc} = \frac{Ei}{ZII} \text{Ib} \quad \text{(II.5)}$$

where I_{SC} is the fault current for bus i and E_i is the voltage before the fault for bus I, which is usually assumed to be 1 p.u. The diagonal member of the impedance matrix is $Z_{ii.}$ Finally, I_b provides the base current. [30].

$$Z_{xy}^{new} = Z_{xy}^{new} - (Z_{xj} - Z_{xk}).(Z_{JY-Z_{ky}})/(Z_{jj+} Z_{kk} - 2Z_{JK+}\text{Zb}) \quad \text{(II.6)}$$

where Z_{new} is the impedance matrix's modified element As a conclusion, inserting the impedance Z_b series with the transmission line has the same effect as inserting the impedance Z_p parallel with the transmission line, as seen by the xy solution.

$$Z_p = (-Zb)//(Z_b + Z_{fcl}) = -Z_b(Z_b + Z_{fcl})/Z_{fcl} \quad \text{(II.7)}$$

When impedance Z_b is added between two buses, the Thevenin equivalent from

the bus understudy can be seen in Fig. 1. Finally, the following expression is used to alter the elements of the impedance matrix:

$$\Delta z_{ii} = -\frac{(z_{ij}-z_{ik})2}{z_{jj}+z_{kk}-2z_{jk}+z_p}\frac{c2}{c1+z_p} \quad \text{(II.8)}$$

Hence the amount of Z_p required to reduce the fault current from Ii, to $Ii_{,F}$ can be calculated from:

$$z_p = \frac{I_{iF}.c2}{(I_{i,n}-I_{i,F}).z_{ii}} - c1 \quad \text{(II.9)}$$

Finally the impedance of the used fault current limiter is

$$z_{fcl} = -\frac{z_b^2}{z_b} + z_p \quad \text{(II.10)}$$

Fault current minimization

The goal of this work is to reduce the fault current at each bus and the fault current can flow over lines to that level. This aim is achieved by installing suitable fault current limiters (FCLs) in the system. To lower financial costs, the overall impedance used for fault current limiters should be minimized. As a conclusion, the problem can be stated as follows:

$$\text{Min } f_1(x) = I_{SC} = \frac{Ei}{ZII} * I_b + Pf_1 \quad \text{(II.11)}$$

where Zii represents the diagonal impedance of the impedance matrix $Zbus$ after inserting FCLs to the system. pfI represents the penalty factor and is defined as follows:

$$\begin{aligned} &if \quad I_j^{sc} \le I_j^{sc,max} \quad j = 1,\ldots,N_b \\ &P_{f1} = 0 \quad \text{(II.12)} \\ &else \quad pf_1 = 500 \times \left(\left|I_j^{sc} - I_j^{sc,max}\right|\right) \end{aligned}$$

Economic aspects of fault current limiter

$$f_2(x) = \frac{\sum_{i=1}^{N_{FCL}} Z_{i,fcl} - Z_{fcl}^{expected}}{Z_{fcl}^{expected}} + Pfz \quad \text{(II.13)}$$

$$f_3(x) = \frac{N_{fcl} - N_{fcl}^{expected}}{N_{fcl}^{expected}} \quad \text{(II.14)}$$

Where $Z_{i,fcl}$ and N_{fcl} are the impedance of the i_{th} FCL and the number of the FCLs in the system, respectively. The parameters $Z_{fcl}^{expected}$ and $N_{fcl}^{expected}$ represent the

anticipated impedance and number of FCLs injected into in the system, respectively. Expected impedance and expected number of FCLs are taken into account while normalizing their related cost functions. These characteristics predict the needed number of FCLs and impedances. Furthermore, pf_z is the penalty factor which is defined as follows:

$$\begin{aligned} &if\ Z_{i,fcl}^{min} \leq Z_{i,fcl} \leq Z_{i,fcl}^{max} \quad i = 1, \ldots, N_{fcl} \\ &\qquad then\ pf_z = 0 \\ &else \quad pf_z = max\left(\left(Z_{i,fcl} - Z_{i,fcl}^{min}\right), \left(Z_{i,fcl}^{max} - Z_{i,fcl}\right)\right) \end{aligned} \tag{II.15}$$

Multi-objective Particle Swarm Optimization (MOPSO).

The proposed method-based on MOPSO [31]. In MOPSO, a particle moves toward one of known Pareto solutions and searches around the solution exploitatively. MOPSO manages Pareto optimal solutions by storing a grid-structured archive [31], [32-33]. Dividing the objective space into hypercubes allows maintaining the diversity of Pareto solutions.

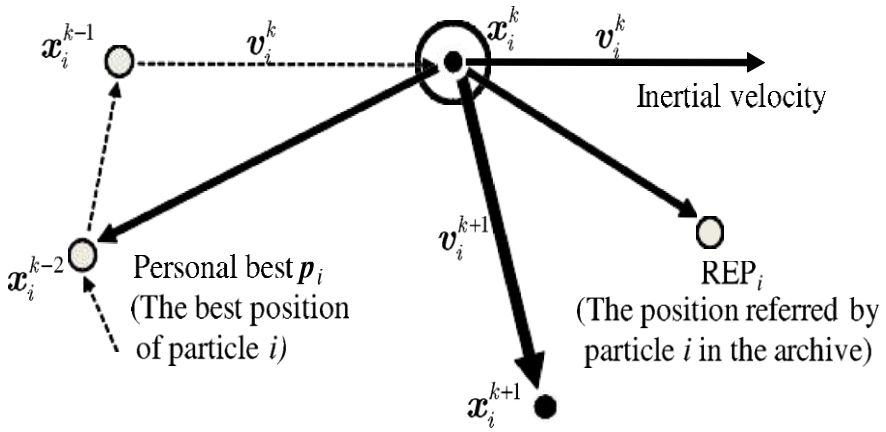

Figure II.2. Velocity and position update

Search by MOPSO

In continue, each particle I is initialized, with its position xi and velocity vi determined at random. The archive is then initialized by storing Pareto solutions derived from a set of positions chosen at random from the search space. At random, each position in the archive is assigned to a particle as REPi. By dividing each objective function into d equal divisions, the objective space is divided on to hyper cubes. xi resets the personal best pi.

After initialization, the proposed algorithm time pad the position and velocity of both the particles. As seen in Figure 3, particle velocity is updated in the archive with its personal best position and referring solution that use the following equation:

$$Vi^{k+1} = \omega vi^{k} + c_1 r_1 \left(X_{pbest_i} - X_i\right) + c_2 r_2 \left(X_{gbest_i} - X_i\right) \quad \text{(II.16)}$$

$$X_i^{k+1} = X_i^k + V_i^{k+1} \quad \text{(II.17)}$$

where X_i^k and V_i^k indicate position and velocity of particle i at step k. X_{pbest_i} indicates personal best of particle i which is the best position of all positions the particle passed so far, X_{gbest_i} is a solution in archive which is referred by particle i. c_1 and c_2 are two positive constants called cognitive and social parameter, r_1 and r_2 are random numbers uniformly distributed within [0, 1].

Particle i is evaluated in its current position $X^{k+1}{}_{i.}$ if $X^{k+1}{}_{i.}$ dominates personal best X_{pbest_i} of particle i, then the position replaces X_{pbest_i}. If neither of the current position nor X_{pbest_i} is dominated by the other, X_{pbest_i} is selected from the m randomly Particle i is reset when it violates the constraint, i.e., it sticks out of the defined variable domain.

Particle i is also reinitialized when satisfying following two conditions:

- Particle i moves too slowly, i.e., its speed v_i goes down under a threshold T_v.
- There has been no improvement on X_{pbest_i} for more than Tr steps.

The outline of the proposed MOPSO

Step 1: Initialize all particles; place them at random positions with random velocities.

Step 2: Evaluate all particle.

Step 3: Store Pareto solutions chosen randomly into the archive.

Step 4: Divide objective function space into hypercubes.

Step 5: Determine personal bests of all solutions.

Step 6: until evaluation, time reaches the limit, *repeat* **step 7**

Step 7: For each particle i, repeat **step 8** through **12**.

Step 9: If *i* moves too slowly, reset its position and velocity.

Step 10: Evaluate *i*.

Step 11: Update personal best and the archive.

Step 12: Redevise the hypercube if necessary.

Optimization procedure

1. According to network data, the impedance matrix of the system Z_{bus} is created.
2. Three phase short circuit fault is applied to all buses.
3. In this research, three objective functions are considered: Short circuit current minimization, number of FCLs, and impedances of FCLs which are installed.

These objective functions are nonlinear and are functions of X. X is the vector of control variables, which is 2n-dimensional vector which represents the location and impedance of

$$X = [X_1, X_2] \qquad X_1 = [sl_1, sl_2, \dots, sl_n] \qquad X_2 = [Z_{1,fcl}, Z_{2,fcl}, \dots, Z_{n,fcl}]$$

FCLs and n is the number of the lines in the network.

sl_i is either one or zero whose value indicates the existence or absence of FCL in i_{th} line.

4. Aforementioned objective functions are functions of X. The MOPSO algorithm is implemented on these objective functions. A penalty term is used based on the safety margin of short circuit current. The proposed optimization procedure determines the location of FCLs and their corresponding values. General procedure flowchart is depicted in Fig. II. 3.

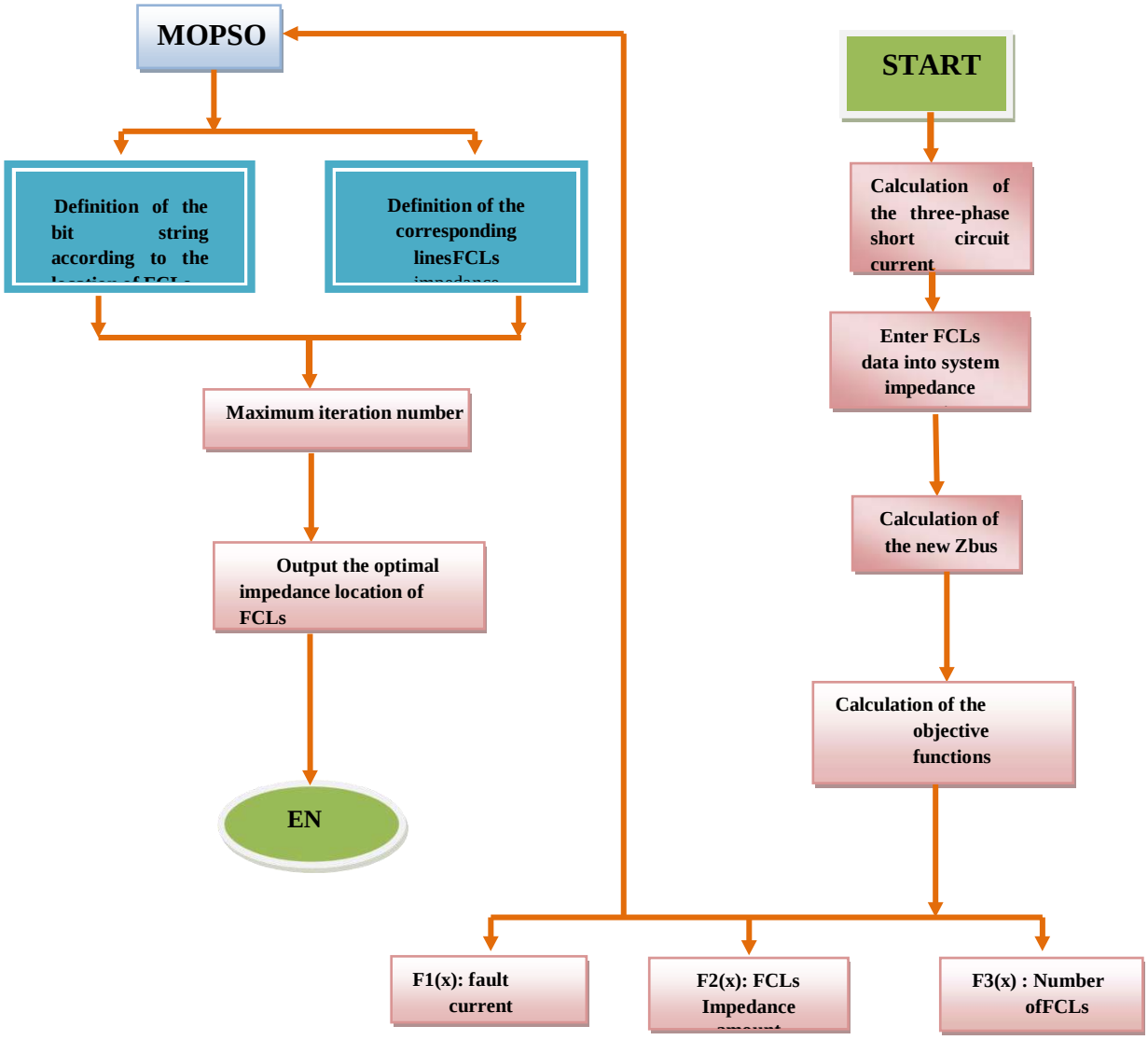

Figure. II.3. General Flowchart of the proposed optimum FCL allocation.

II.5 Conclusion

In this part of the work, we have studied both the fault current calculation and the effect of adding a FCL on Z_{BUS} impedance and number of FCLs, and we have extracted all the expressions and their optimal solutions.

Multiobjective particle swarm optimization applied in IEEE 30-bus system is study in chapter 3 to short circuit fault current reduction. Simulation results and discussion are presented in the same chapter.

Chapter III

Simulation results and discussions

Introduction

In this work, we applied a Pareto based optimization algorithm, namely multi-objective particle swarm optimization MOPSO in IEEE 30-bus test system. The test system has 06 generators, 24 load buses and 41 transmission lines. The single line diagram of the test system is depicted in Figeur (III.1).

Simulation results

The problem of FCL optimal allocation is a nonlinear optimization problem, and may include several objective functions. In this study, objective functions considered are as short circuit current reduction, and the economical usage of FCLs. These objective functions are explained in the previous chapter.

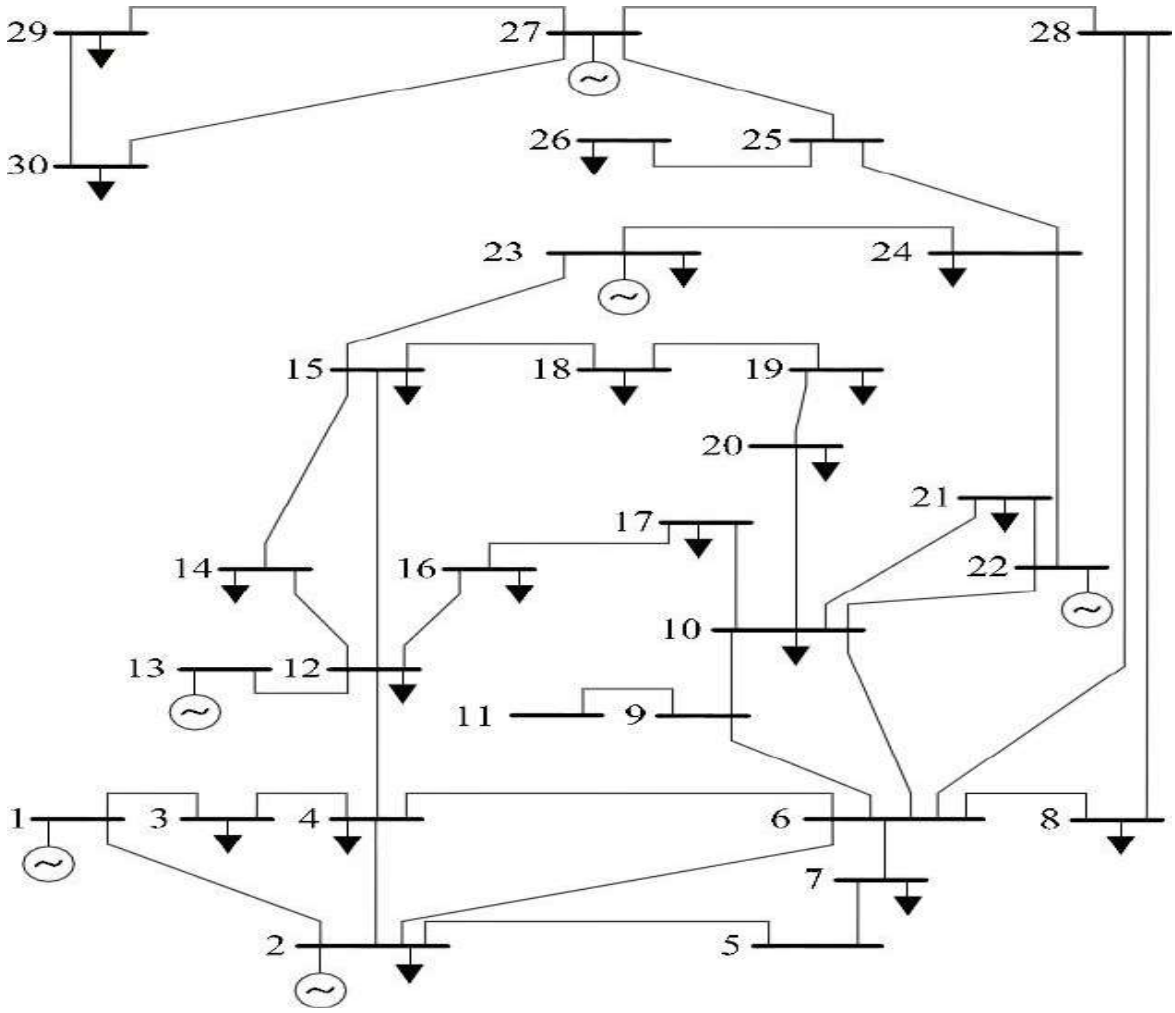

Figure III.1: Single line diagram of the IEEE 30-bus test system

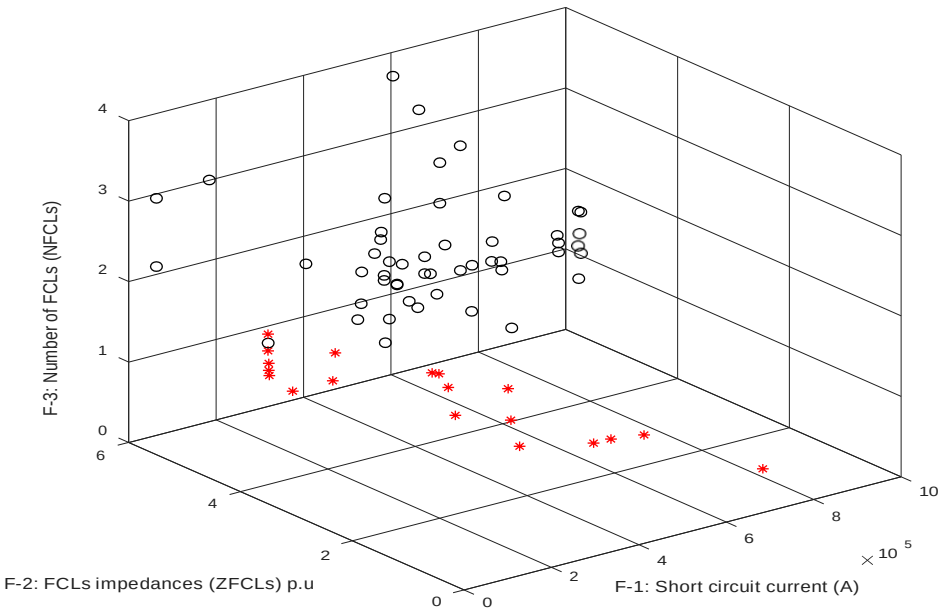

Figure III.2: MOPSO algorithm Pareto front for IEEE 30-bus system.

Figure III.2 represent the Pareto front obtained by MOPSO algorithm for IEEE 30 Bus system. Fig. III.3 demonstrate the compare fault current before and after installation of SFCLs.

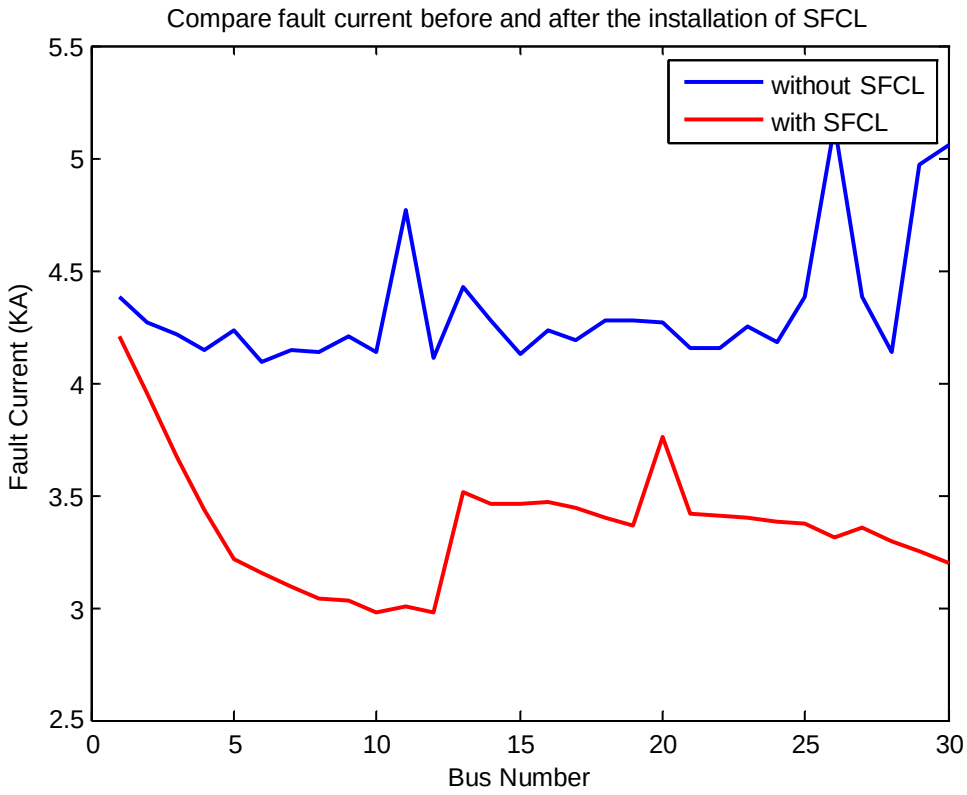

Figure III.3: Compare fault current before and after installation of SFCL.

Table III.1: Compare fault current before and after installation SFCL.

Bus Number	I_{FCLs} Before (A)	I_{FCLs} After (A)	Reduction Percent (%)
1	4.3841	4.2037	4.1148
2	4.2657	3.9376	7.6916
3	4.2150	3.6370	13.7129
4	4.1416	3.3591	18.8936
5	4.2316	3.1543	25.4584
6	4.0935	3.0862	24.6073
7	4.1472	3.0315	26.9025
8	4.1375	2.9788	28.0048
9	4.2062	2.9598	29.6324
10	4.1392	2.9040	29.8415
11	4.7667	2.9277	38.5801
12	4.1076	2.9115	29.1192
13	4.4253	3.4519	21.1059
14	4.2773	3.3991	20.5316
15	4.1282	3.3954	177.5108
16	4.2302	3.4041	19.5286
17	4.1868	3.3857	19.1339
18	4.2729	3.3448	21.7206
19	4.2755	3.3098	27.5406
20	4.2698	3.7376	12.4643
21	4.1508	3.3559	19.1505
22	4.1531	3.3466	19.4192
23	4.2514	3.3363	21.5247
24	4.1806	3.3218	205.4251
25	4.3817	3.3105	24.4471
26	5.1457	3.2506	36.8288
27	4.3824	3.2926	25.0753
28	4.1347	3.2276	21.9387
29	4.9660	3.1903	3.57571
30	5.0560	3.1350	37.9944

Table III.1 gives fault current before and after installation of SFCLs, and the reduction percent. As can be seen from the table, SFCL helps to manage economically this fault current to avoid damages to equipment, which can result in blackouts. SFCLs does not suppress the fault current completely, but rather reduces the fault current to a level that the equipment or devices can withstand. The best (optimal) values of short circuit fault current, Economical aspects use of FCL (impedance and number of FCLs) obtained by MOPSO are 65,5033 (A), 1.5013 p.u, and 4, respectively.

Fig. III.4 illustrates graphic representation (bar) of compare fault current before and after installation of SFCLs. Figure (III.5) shows graphic representation (bar) of reduction percent between short circuit faults current before and after installation of SFCLs on IEEE 30 bus system.

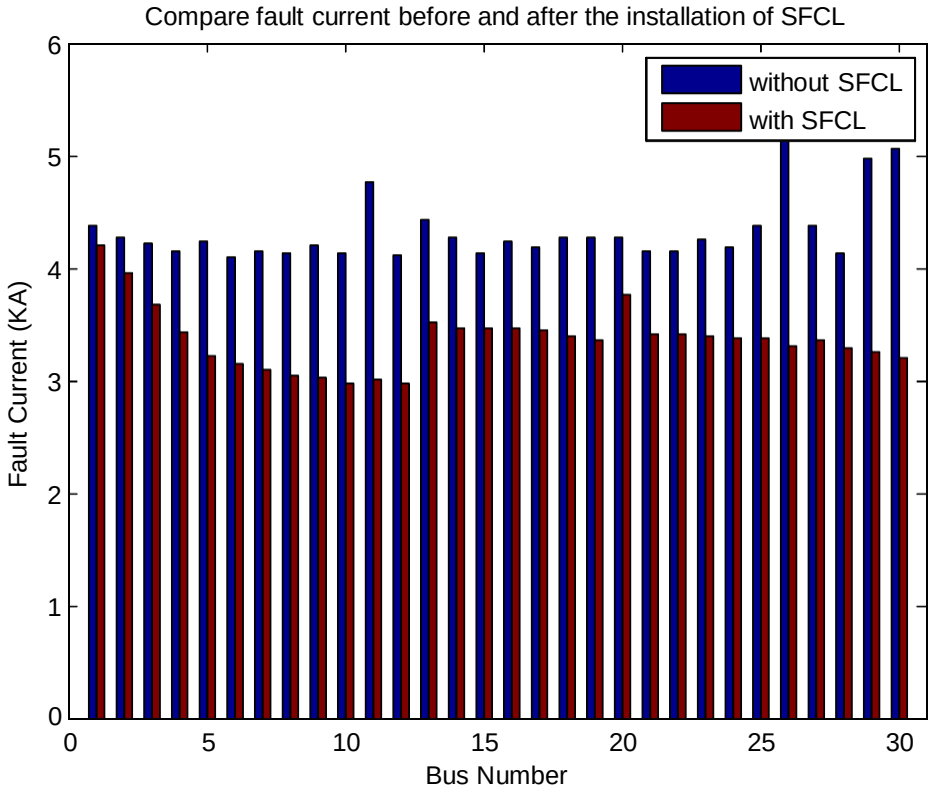

Figure III.4: Compare fault current before and after installation SFCL.

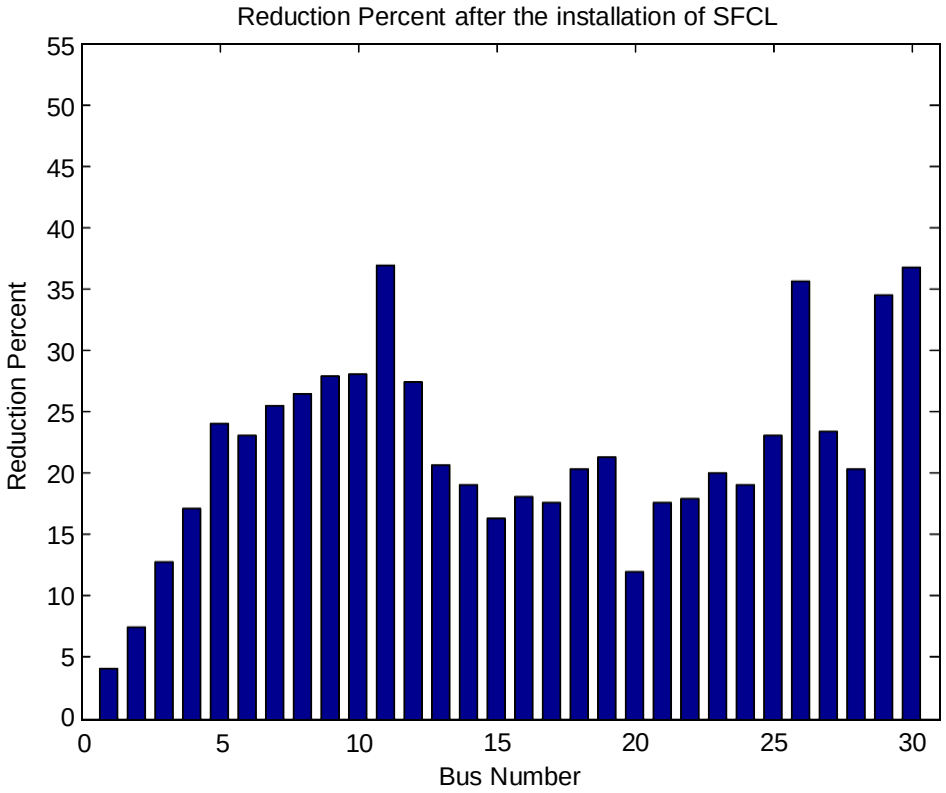

Figure III.5: Reduction percent of fault current after the installation of SFCL.

Table III.2: Magnitude voltages of buses before and after installation SFCL.

Buses	Initial magnitude voltage before installing SFCL(pu)	Magnitude voltage after installing SFCL(pu)
1	**1,0600**	**1.0600**
2	1,0430	1.0430
3	1.0000	1.0215
4	1,0600	1.0129
5	1,0100	1.0100
6	1.0000	1.0121
7	1.0000	1.0034
8	1,0100	1.0100
9	1.0000	1.0510
10	1.0000	1.0444
11	1,0820	1.0820
12	1.0000	1.0574
13	1,0710	1.0710
14	1.0000	1.0424
15	1.0000	1.0378
16	1.0000	1.0447
17	1.0000	1.0391
18	1.0000	1.0279
19	1.0000	1.0253
20	1.0000	1.0293
21	1.0000	1.0321
22	1.0000	1.0327
23	1.0000	1.0272
24	1.0000	1.0216
25	1.0000	1.0189
26	1.0000	1.0012
27	1.0000	1.0257
28	1.0000	1.0107
29	1.0000	1.0059
30	1.0000	0.9945

Table III.2 represent magnitude voltages of buses before and after installation SFCL.

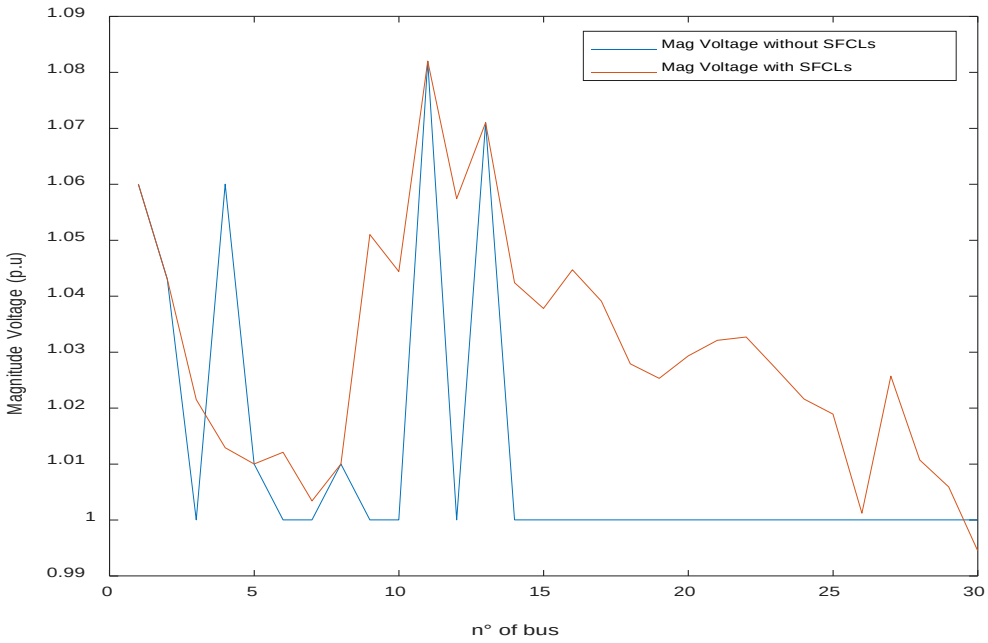

Figure III.6: Voltage profile of IEEE 30 bus system without and with SFCLs installation.

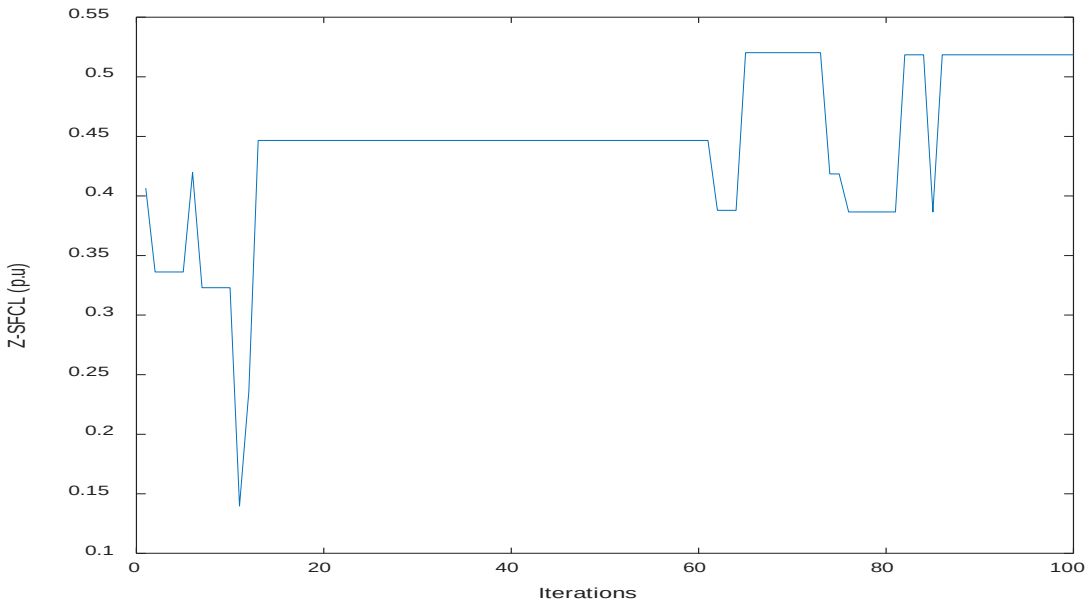

Figure III.7: Variation of Z_{SFCL} with iterations.

Figure III.6 shows the voltage profile of IEEE 30 bus system without and with installation of SFCLs.

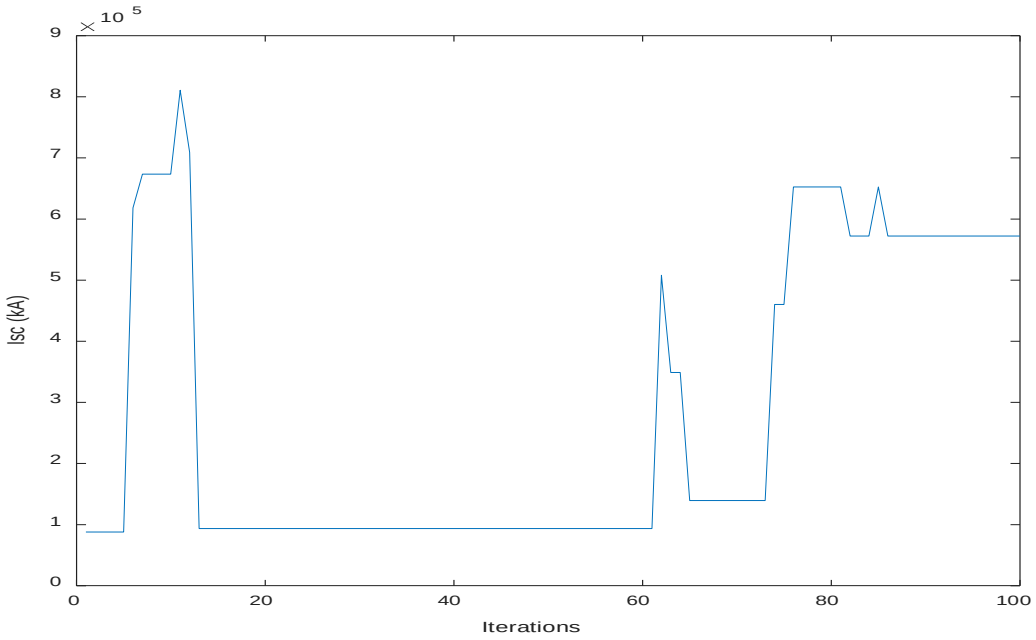

Figure III.8: Variation of short circuit fault current (I_{SC}) with iterations.

Table III.4 : Variable control values.

FCL installation candidate lines	10, 19, 26, 15, 20, 21
FCLs impedance corresponding to above installation locations	0.1754, 0.3112, 0.4304, 0.5843, 0.2837, 0.2695
Number of installed FCLs	**6**

Table III.5 : Optimal values.

Isc	6.5033 10^4 (A)
Impedance of FCLs	1.5013
Number of FCLs	4

Table III.4 represent a typical solution from the Pareto fronts obtained by MOPSO. As can be seen from the table, using MOPSO algorithm totally 2.0545 p.u limiting impedances are inserted in the range of 0.1754-0.5843 p.u to 6 lines of the network.

III.3 Conclusion

The insertion of FCLs to a power system has a massive effect on short circuit current suppression. However, how FCL is installing, short circuit current is depending on installation sites and impedances. The MOPSO algorithm used in this work is based on the idea of dominance and produces a Pareto front. MOPSO is the algorithm involved. The cost functions take account adaptive penalty factors for short circuit current limiting violations and FCL impedance margins.

General Conclusion

General Conclusion

The installation of FCLs into a power system has a great effect on short circuit current elimination and power system enhanced. However, how installing FCLs, the short circuit current depends on the installation locations and their impedances. The existing approaches in literature use weighted sum of different objective functions to obtain a single objective problem and then apply single objective optimization algorithms to it. Moreover, to the best knowledge of the authors; there does not exist any reported simultaneous structure and parameter value optimization in the allocation problem of FCLs.

In this thesis, MOPSO approach is proposed on IEEE 30-bus system to obtain installation locations, impedance and the number of FCLs, simultaneously. The MOPSO technique used in this work is based on dominance concept and result in a Pareto front. An adaptive penalty factors for the violation of short circuit current limitation and FCLs impedance margins are considered in the cost functions. One of the main advantages of the proposed approach is that using the proposed method, it is possible to optimize the location and the values of FCLs, simultaneously. Moreover, a lower bound for the short circuit current of the power system is considered which reduces the need for FCLs, which causes less cost for the whole system.

It is worth noting that since the placement and the value of the impedances of the FCLs affect the operation time of directional overcurrent relays, it can be considered as a new objective function. We consider this objective function as a new research topic in future.

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